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# Order Statistics Based Low-Power Flash ADC with On-Chip Comparator Selection

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**SUMMARY** High-speed flash ADCs are useful in high-speed applications such as communication receivers. Due to offset voltage variation in the sub-micron processes, the power consumption and the area increase significantly to suppress variation. As an alternative to suppressing the variation, we have developed a flash ADC architecture that selects the comparators based on offset voltage ranking for reference generation. Specifically, with the order statistics as a basis, our method selects the minimum number of comparators to obtain equally spaced reference values. Because the proposed ADC utilizes offset voltages as references, no resistor ladder is required. We also developed a time-domain sorting mechanism for the offset voltages to achieve on-chip comparator selection. We first perform a detailed analysis of the order statistics based selection method and then design a 4-bit ADC in a commercial 65-nm process and perform transistor-level simulation. When using 127 comparators, INLs of 20 virtual chips are in the range of −0.34 LSB/+0.29 LSB to −0.83 LSB/+0.74 LSB, and DNLs are in the range of −0.33 LSB/+0.24 LSB to −0.77 LSB/+1.18 LSB at 1-GS/s operation. Our ADC achieves the SNDR of 20.9 dB at Nyquist-frequency input and the power consumption of 0.84 mW.

***key words:*** *flash ADC, offset voltage, order statistics, on-chip calibration*

## 1. Introduction

High-speed flash ADCs are useful in high-speed applications such as communication receivers. However, due to the increase of random mismatch in the sub-micron processes, it is difficult to achieve both a small area and low-power operation. To achieve high linearity, comparators with small offset voltage variation and accurate reference generation are required. Up-sized MOSFETs or offset cancellation techniques are generally employed to reduce offset voltage variation. Since up-sized MOSFETs have large parasitic capacitances, power consumption increases accordingly. Offset cancellations require additional capacitors and switches to compensate for the offset voltage and can be used only for continuous comparators or latched comparators with preamps. However, because these techniques require high gain amplifiers, power consumption increases [1], [2]. Instead of cancelling the offset voltage by sampling, several offset tuning mechanisms have been proposed as low-power solutions [3]–[7].

As an alternative to cancelling or tuning the offset voltage, flash ADC architectures that utilize the offset voltage variation to eliminate the need for a resistor ladder have been proposed [8]–[13]. One of these methods is stochastic flash ADC [8]–[11]. Since these ADCs obtain the conversion results from the cumulative distribution function (CDF), near minimum-size comparators can be used. Therefore, power consumption in each of the comparators can be reduced significantly compared to that in a typical flash ADC architecture. However, all the redundant comparators need to operate in the stochastic architecture, which results in an increase of power and kickback noise. The small input voltage range is also a problem due to the limited linear region of CDF. To increase the range of the linear region, methods of shifting and swapping the offset voltage distributions have been proposed [9], [10]. However, these methods require more comparators, which leads to additional power consumption. As stochastic ADCs sum up the outputs of all the comparators, an increase in the comparator number not only increases the comparator power and kickback noise but also the power required for the adder. Flash ADCs that select the minimum number of comparators to obtain equally spaced offset voltages by measuring the offset voltages directly have been proposed [12]–[14]. Although these flash ADCs can reduce the number of active comparators, voltage sweep with known values is required in this case. Although analog voltages can be generated by on-chip DACs, the linearity of the DACs will affect the accuracy of the comparator selection.

As a calibration method to eliminate the need for DACs, we previously proposed a flash ADC architecture that selects comparators based on the rankings of the offset voltages [15]. By calculating the rankings from the distribution of offset voltages based on order statistics, equally spaced offset voltages can be obtained. Since comparators are selected by their relative offset voltage values, only a monotonic increase or decrease of the input voltage is sufficient during calibration. Thus, the ranking estimation can be achieved by time-domain measurements, which can easily be implemented on-chip. This paper is an extension of our prior work [15] with the following additional contents.

1. Improving the accuracy of ranking estimation by tuning the input capacitance dynamically.
2. Simulating multiple virtual chips to assess the range of DNL and INL.
3. Evaluating the dynamic characteristics of SNDR based on a noise transient analysis.

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In this paper, we first verify our proposed order statistics based selection by performing theoretical analysis. We then present a design example of a 4-bit flash ADC including an on-chip calibration mechanism. We verify our proposed architecture by HSPICE [16] simulation based on a commercial 65-nm general-purpose process and evaluate the ADC performance. In the case of using 127 comparators, INLs of 20 virtual chips are in the range of −0.34 LSB/+0.29 LSB to −0.83 LSB/+0.74 LSB, and DNLs are in the range of −0.33 LSB/+0.24 LSB to −0.77 LSB/+1.18 LSB. We also evaluate the dynamic characteristics by conducting noise transient analysis under thermal noise. Our ADC achieves the SNDR of 20.9 dB at Nyquist-frequency input and the power consumption of 0.84 mW, resulting in the FoM of 93 fJ/conv.

In Sect. 2 of this paper, we present our order statistics based flash ADC along with an on-chip sorting mechanism. Section 3 demonstrates some theoretical analysis of the proposed ADC. In Sect. 4, we present a design example of a 4-bit ADC using our proposed technique. In Sect. 5, we verify our ADC by transistor-level simulations. We conclude in Sect. 6 with a brief summary.

## 2. Order Statistics Based Flash ADC

### 2.1 Concept

Our proposed flash ADC utilizes offset voltages as references. Figure 1 shows the structure of this flash ADC. Our method selects $2^N - 1$ comparators whose offset voltages are equally spaced to obtain the voltage references as shown in Fig. 2, where $N$ is the resolution of the ADC. The selection is performed based on the rankings of offset voltages. The target rankings are calculated based on order statistics. After activating the selected comparators only, AD conversion is achieved by summing up the comparator outputs. The unused comparators do not consume dynamic power as they are turned off. Furthermore, as we can design the comparators with near-minimum size transistors, area overhead due to the redundant comparators is also small.

### 2.2 Order Statistics Based Comparator Selection

Our proposed ADC selects the comparators from the rankings of offset voltages to obtain equally spaced voltage references. We estimate the required rankings to obtain equally spaced reference voltages using order statistics. Order statistics are ordered samples shown as follows.

$$V_{(1)} \le V_{(2)} \le \cdots \le V_{(k)} \le \cdots \le V_{(n)}. \tag{1}$$

$V_{(k)}$ is said to be the $k$-th order statistic. To distinguish unordered samples from ordered samples strictly, we show unordered samples of offset voltage as $v$ and ordered samples as $v_{(k)}$. Using a probability density function (PDF) $f(v)$ and a CDF $F(v)$ of an unordered-sample distribution, a PDF $f_{V_{(k)}}(v_{(k)})$ and a CDF $F_{V_{(k)}}(v_{(k)})$ of $k$-th order statistic are

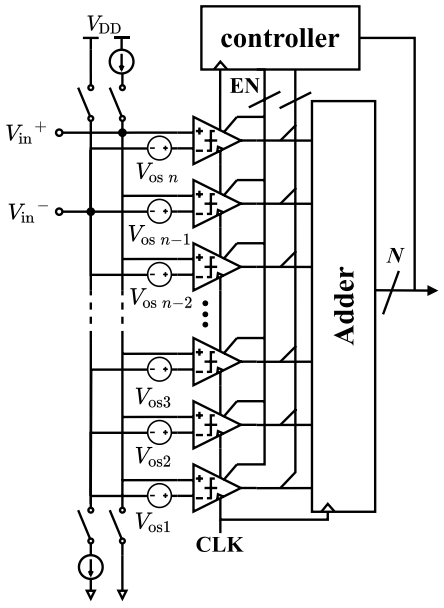


**Fig. 1** Structure of order statistics based flash ADC.

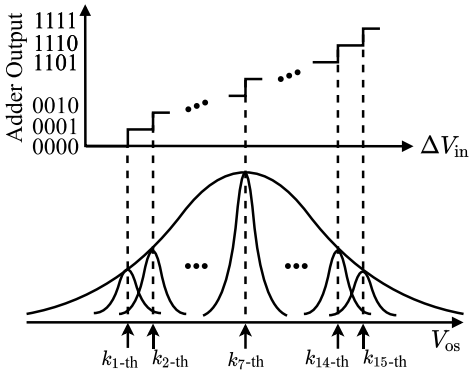


**Fig. 2** Concept of order statistics based flash ADC.

respectively calculated as follows [17].

$$F_{V_{(k)}}(v_{(k)}) = \sum_{l=k}^{n} {}_n\mathrm{C}_l F(v_{(k)})^l (1 - F(v_{(k)}))^{n-l}, \tag{2}$$

$$f_{V_{(k)}}(v_{(k)}) = \frac{n! F(v_{(k)})^{k-1} \left\{1 - F(v_{(k)})\right\}^{n-k} f(v_{(k)})}{(k-1)!(n-k)!}. \tag{3}$$

Here, $n$ shows the number of comparators. From Eq. (2), we can obtain the median of the $k$-th order statistic as

$$V_{\mathrm{m}} = F^{-1}_{V_{(k)}}(0.5). \tag{4}$$

After calculating the median voltage $V_{\mathrm{m}}$ for all $k$, we select the ranking whose median voltage is closest to the target voltage $V_{\mathrm{T}}$. In this way, we calculate the rankings $k_1, k_2, \cdots, k_{2^N-1}$ for each target voltage $V_{\mathrm{T}1}$, $V_{\mathrm{T}2}$, $\cdots$, $V_{\mathrm{T}2^N-1}$. By selecting comparators based on the calculated rankings, equally spaced offset voltages are obtained. Then, by counting the outputs of the selected comparators, AD conversion is achieved.

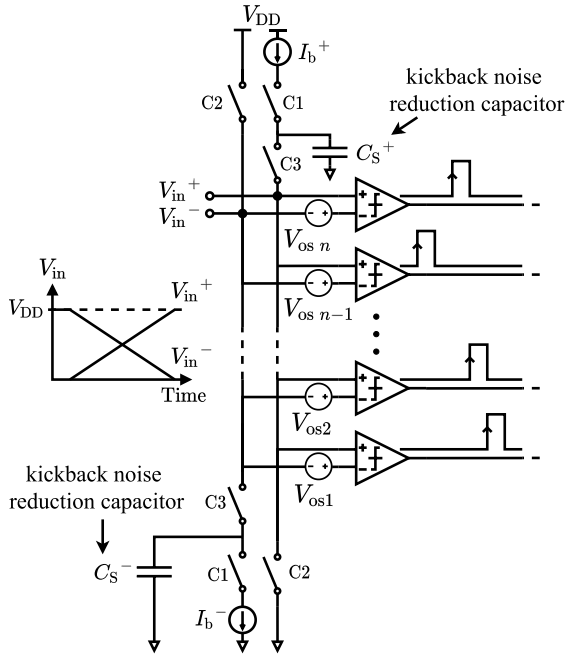


**Fig. 3** Proposed on-chip mechanism for offset voltage ranking estimation.

### 2.3 On-Chip Sorting Mechanism

The proposed ADC selects the comparators from the pre-calculated rankings of offset voltages. We now propose an on-chip sorting mechanism that can estimate the offset voltage rankings, as shown in Fig. 3. The sorting operation is conducted as follows. First, the node $V_{in}^+$ is pulled down to $V_{SS}$ and the node $V_{in}^-$ is pulled up to $V_{DD}$. Then, the node $V_{in}^+$ is charged and the node $V_{in}^-$ is discharged simultaneously by current sources, and the outputs of the comparators are sampled per clock. Because comparators with low offset voltage are inverted earlier than others, we can estimate the rankings from each comparator's time to activate. Since the ADC uses only the relative relationship between the offset voltages, a simple current source based implementation is enough to generate the voltage differences. In addition, since only a monotonic increase or decrease of voltages is sufficient to obtain the offset voltage ranking, fixed values of the current sources are not necessary. Hence, the current sources for the ranking estimation do not require accurate references. The requirement for the current value is $I_b \leq V_{res} C_{in} f_{clk}$, where $V_{res}$ is the voltage resolution required to estimate the ranking with sufficient accuracy.

During the sorting operation, all the comparators need to be active. As a result, kickback noise from the comparators is larger than that during AD conversion, where only $2^N - 1$ comparators operate. This difference in the noise level may degrade the accuracy of the ranking estimation. To ensure the sorting accuracy, we insert additional input capacitors $C_S^+$ and $C_S^-$ to suppress the additional noise. These capacitors are enabled only during the sorting operation and are disabled during AD conversion to reduce the input capacitance.

Flash ADCs in which offset voltages are used as references or are tuned may suffer from offset voltage variation at different temperatures or supply voltages. To deal with this issue, re-calibration can be performed periodically or based on the instruction from the system.

## 3. Theoretical Analysis of Proposed ADC

In this section, we evaluate the linearity of the proposed ADC theoretically to determine the required comparator number that enables the target linearity to be achieved.

### 3.1 Worst-Case INL

First, we derive the integral non-linearity (INL) of the proposed ADC using order statistics. INL[$i$] is defined as

$$\mathrm{INL}[i] = \frac{V_{(k_i)} - V_{Ti}}{V_{LSB}}. \tag{5}$$

To systematically evaluate the worst-case INL, we adopt the end-point definition in the analysis. During the evaluation of an actual ADC, we use the best-fit definition, which gives a better result compared to the end-point definition [18]. The PDF $f_{V_{(k_i)}}(v_{(k_i)})$ and the CDF $F_{V_{(k_i)}}(v_{(k_i)})$ of the $k_i$-th order statistic are obtained by Eqs. (2) and (3). To derive these distributions, the original distribution of offset voltage is required. By using the well-defined variation models of MOSFETs, we can pre-simulate the distribution of the offset voltage. Thus, we can obtain the order statistic distribution by substituting the PDF $f(v)$ and the CDF $F(v)$ of the unordered offset voltage to Eqs. (2) and (3). From the CDF of the $k_i$-th order statistic, we can obtain $v_{\min(k_i)}$ and $v_{\max(k_i)}$, which satisfy the following equation for each $i$.

$$v_{\min(k_i)} = F_{k_i}^{-1}(0.025), v_{\max(k_i)} = F_{k_i}^{-1}(0.975). \tag{6}$$

Then, we can calculate the 95% interval of INL[$i$] as follows.

$$\frac{V_{\min(k_i)} - V_{Ti}}{V_{LSB}} < \mathrm{INL}[i] < \frac{V_{\max(k_i)} - V_{Ti}}{V_{LSB}}. \tag{7}$$

Using the above result, we evaluate the relationship between INL and the number of comparators. Since the threshold voltage of MOSFETs follows a normal distribution [19], we perform the analysis assuming that offset voltage also follows a normal distribution. Substituting the PDF and the CDF of the normal distribution to Eq. (2), confidence intervals of INL[$i$] for all $i$ can be calculated numerically. After that, we evaluate min {INL[$i$]} and max {INL[$i$]}. Figure 4 shows the relationship between INL and the number of comparators when the input range is set as $3\sigma_{os}$ for different bit numbers, where $\sigma_{os}$ is the standard derivation of offset voltage. With the increase of ADC resolution, more comparators are required to achieve the same level of INL. When using 127 comparators to achieve a 4-bit ADC, INL is within −1.80 LSB/+1.77 LSB.

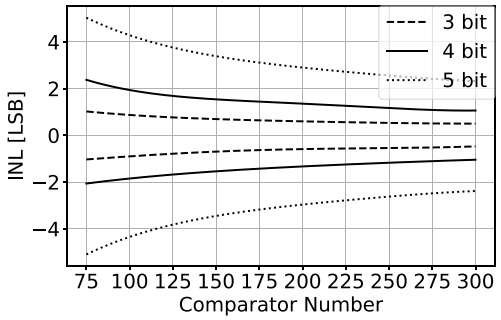


**Fig. 4** Relation between INL and comparator number.

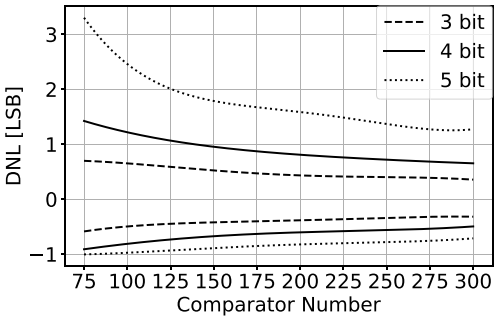


**Fig. 5** Relation between DNL and comparator number.

### 3.2 Worst-Case DNL

Differential non-linearity (DNL) of the proposed ADC can be evaluated using the distribution of the difference $W_i = V_{(k_{i+1})} - V_{(k_i)}$. The PDF $g_i(w_i)$ and the CDF $G_i(w_i)$ of $w_i$ are obtained as follows [17].

$$g_i(w_i) = \frac{n!}{(k_i-1)!(k_{i+1}-k_i-1)!(n-k_{i+1})!} \cdot \int_{-\infty}^{\infty} F(v_{(k_i)})^{k_i-1}(F(v_{(k_i)}+w_i)-F(v_{(k_i)}))^{k_{i+1}-k_i-1} \cdot (1-F(v_{(k_i)}+w_i))^{n-k_{i+1}} f(v_{(k_i)}) f(v_{(k_i)}+w_i) \mathrm{d}v_{(k_i)} \ . \quad (8)$$

$$G_i(w_i) = \int_0^{w_i} g(w)\mathrm{d}w \ . \quad (9)$$

We can calculate $w_{\min(k_i)}$ and $w_{\max(k_i)}$ that satisfy the following equations for each $i$.

$$w_{\min(k_i)} = G_i^{-1}(0.025), \ w_{\max(k_i)} = G_i^{-1}(0.975) \ . \quad (10)$$

DNL[$i$] then falls within the following range for 95% of the chips.

$$\frac{w_{\min(k_i)}}{V_{\mathrm{LSB}}} - 1 < \mathrm{DNL}[i] < \frac{w_{\max(k_i)}}{V_{\mathrm{LSB}}} - 1 \ . \quad (11)$$

Using the above result, we evaluate the relationship between DNL and the number of comparators. Substituting the PDF and the CDF of the normal distribution, the confidence intervals of DNL[$i$] for all $i$ can be calculated numerically. After that, we evaluate min {DNL[$i$]} and max {DNL[$i$]}. Figure 5 shows the relationship between DNL and the number of comparators when the input range is $3\sigma_{\mathrm{os}}$ for different bit numbers. As the DNL cannot be less than $-1.0$ identically, the outline of the graph is asymmetric to the x-axis. In the case of using 127 comparators to achieve a 4-bit ADC, DNL falls within $-0.71$ LSB/+1.13 LSB under the 95% confidence interval.

## 4. Design Example

### 4.1 Comparator

Figure 6 shows the structure of the comparator including

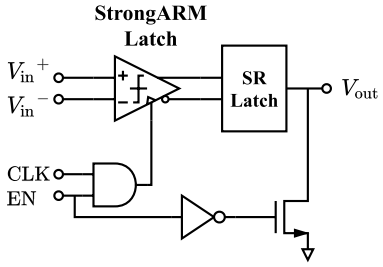


**Fig. 6** Structure of comparator.

the control logic for activation. We use a strongARM latch as the latch stage [20]. This is a synchronous comparator where the comparison result is held only for the half period of one clock cycle. To retain the comparison result during the full clock cycle, an SR-latch is cascaded after the latch stage [21]. Moreover, to disable the unused comparators, an activation circuit is added that stops supplying the clock signal and pulls down the output to low.

Near-minimum size MOSFETs are used for the comparators to obtain large offset voltage variation. Thus, the power consumption of each comparator is low. However, since near-minimum size MOSFETs have a small parasitic capacitance, the comparator suffers significantly from thermal noise. The input-referred noise voltage of the strongARM latch is determined by the capacitances $C_{\mathrm{C}}$ and $C_{\mathrm{L}}$ [22]. To suppress the input-referred voltage noise, we insert additional capacitances as shown in Fig. 8. We avoid increasing the size of the MOSFETs, as this would increase the power consumption of the clock drivers too. We tune the gate widths of M4 to M7 only to make sure that capacitance $C_{\mathrm{L}}$ is sufficiently large. The input-referred voltage noise of our designed strongARM latch is 0.95 mV.

We simulate the offset voltage distribution of the comparators by Monte Carlo analysis considering random mismatch of MOSFETs. A foundry-provided statistical model for the mismatch is used in the simulation. Figure 9 shows the distribution of offset voltage. The average offset voltage is 1.0 mV and the standard deviation $\sigma_{\mathrm{os}}$ is 25.0 mV.

### 4.2 Sorting Mechanism

We propose a sorting mechanism to estimate the rankings for on-chip selection. Figure 10 shows the structure of the

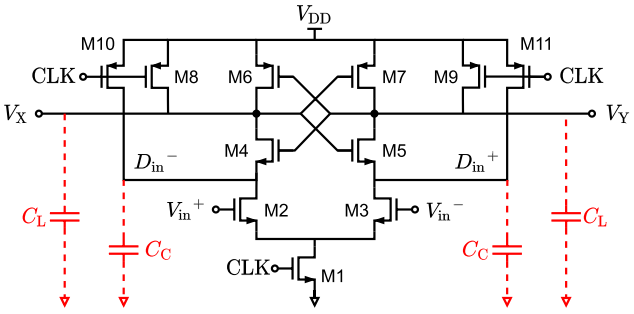


**Fig. 7** StrongARM latch. $C_C$ and $C_L$ are parasitic capacitances.

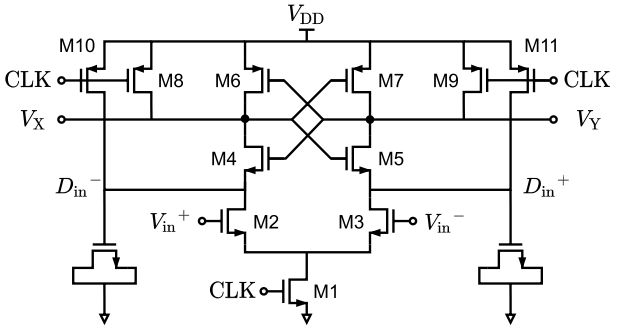


**Fig. 8** StrongARM latch with additional gate capacitances inserted.

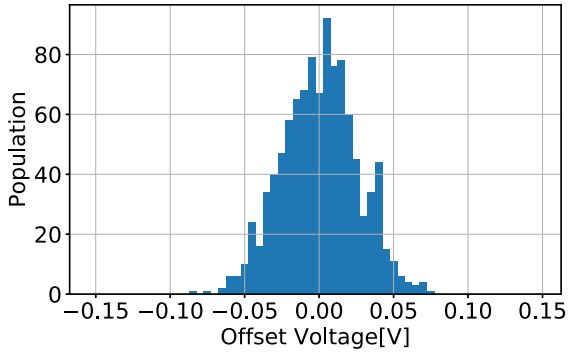


**Fig. 9** Histogram of simulated comparator offset voltage.

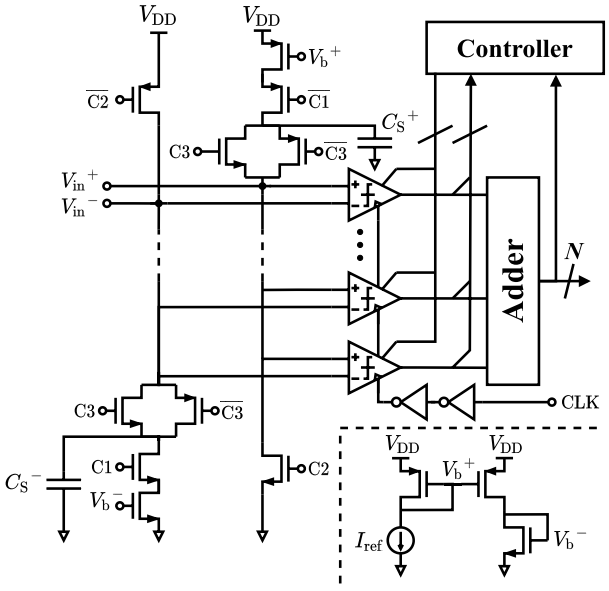


**Fig. 10** Design example of sorting circuit.

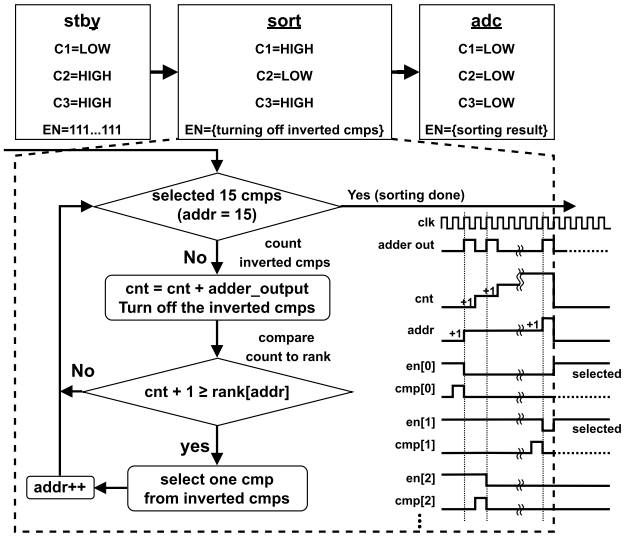


**Fig. 11** Detailed operation of sorting mechanism.

sorting circuit. The current sources are implemented by the MOSFETs with bias voltages $V_b^+$ and $V_b^-$. The switches C1 and C2 are implemented as a single MOSFET, and C3 is implemented as a transmission gate. Figure 11 illustrates the details of the sorting mechanism. Before the sorting operation, the controller sets the C1 to C3 signals appropriately to pull down $V_{in}^+$ to $V_{SS}$ and pull up $V_{in}^-$ to $V_{DD}$ during the standby state. Next, the controller enables the current sources and the kickback reduction capacitors. The input nodes then start to be charged or discharged. The outputs of the comparators are inverted when the differential input voltage becomes larger than their offset voltages. To count the number of comparators that are inverted, the controller disables the comparator after detecting their inverted outputs and accumulates the adder output at every clock cycle. If the accumulated result is larger than a target rank, the controller selects the target comparator whose output was inverted most recently. There is a possibility that multiple comparators will invert their outputs at the same time, so we need a mechanism to select one among the multiple inverted comparators. In our mechanism, the controller checks each comparator's output and selects the first comparator with the inverted output. It repeats this operation until $2^N - 1$ comparators are selected. The values of the target rankings can be set by a serial interface or hard-coded during design. When the controller concludes sorting, it sets the control signals to activate ADC mode.

### 4.3 Adder

A Wallace tree encoder is used to convert comparator output signals to a binary signal. In the case of a stochastic ADC

[12], many comparators operate simultaneously and their output nodes are inverted depending on the input voltage. Therefore, the inputs of the encoder have a high activity rate that results in higher power consumption. Conversely, since only $2^N - 1$ comparators operate in the proposed ADC, switching probabilities of nodes in the encoder are low which results in lower power consumption.

## 5. Simulation Results

We verify our ADC by HSPICE simulation based on transistor models assuming a commercial 65-nm general-purpose process. We evaluate the input and output characteristics of 20 virtual chips using Monte Carlo simulation. Analog components such as comparators and sorting circuits are simulated at the transistor level, while the digital circuits such as the adder and the controller are implemented using a behavioral model. The initial values of $V_{\text{in}}{}^{+}$ and $V_{\text{in}}{}^{-}$ are set to 0.4 V and 0.6 V, respectively to reduce simulation time. The standard derivation of offset voltage $\sigma_{\text{os}}$ is 25.0 mV, and the relation between the selection ranking and the median of offset voltage is shown in Fig. 12. The rankings for equally spaced offset voltages are calculated as 12th, 17th, 23rd, 29th, 37th, 46th, 55th, 64th, 74th, 83rd, 91st, 99th, 106th, 111th, and 116th. Then, the proposed sorting circuit selects 15 comparators from 127 comparators based on the above rankings. In the ADC mode, only 15 comparators are active, while in the sorting mode, 127 comparators are active. Hence, kickback noise during sorting mode will increase by roughly 10 times. Since the input capacitance is about 500 fF, we use additional capacitances $C_{\text{S}}^{+}$ and $C_{\text{S}}^{-}$ of 5 pF to suppress the additional noise. Figure 13 shows the DNL and the INL of 20 chips. INLs of all 20 chips fall in the range of −0.34 LSB/+0.29 LSB to −0.83 LSB/+0.74 LSB, and DNLs are in the range of −0.33 LSB/+0.24 LSB to −0.77 LSB/+1.18 LSB. Next, we evaluate the SNDR of the ADC by a noise transient simulation. Figure 14 shows the simulated waveform of input nodes $V_{\text{in}}{}^{+}$, $V_{\text{in}}{}^{-}$ and the decimal code of the adder output. The calibration is performed in the first half of the simulation. After that, differential sinusoidal waves are applied to the inputs. To prevent over-clipping, the input amplitude is set as −1 dB compared to the full-scale range of ADC [18]. In this result, the ADC achieves an SNDR of 21.0 dB, which results in an ENOB of 3.20 bits. Figure 15 shows the power spectrum of the ADC when the input frequency is 495 MHz. The ADC achieves an SNDR of 20.9 dB and an ENOB of 3.18 bits. The power consumption of the analog components is 0.36 mW. The rest of the circuit components are the adder and the controller. Since the controller is inactive during the AD conversion, we simulate the power consumption of the adder based on the synthesized netlist using Design Compiler [23]. We then estimate the average power consumption by propagating the input switching probability into each node. When setting the toggle rate as 0.5 to 15 inputs out of the 127 inputs, the Wallace tree adder consumes 0.48 mW. The total power consumption thus becomes 0.84 mW. Therefore, the

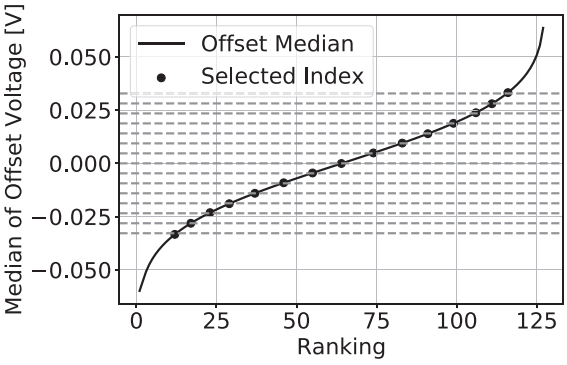


**Fig. 12** Relation between ranking and median of offset voltage.

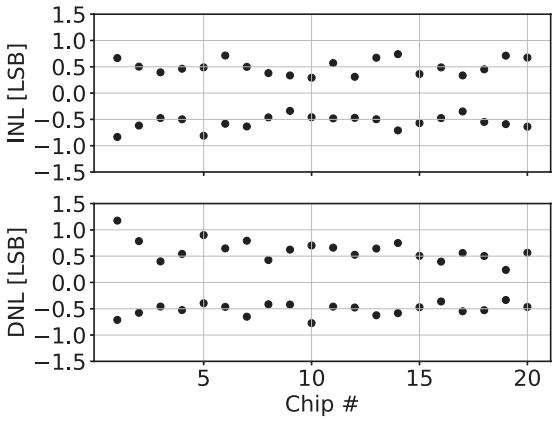


**Fig. 13** Simulated INLs and DNLs of 20 chips.

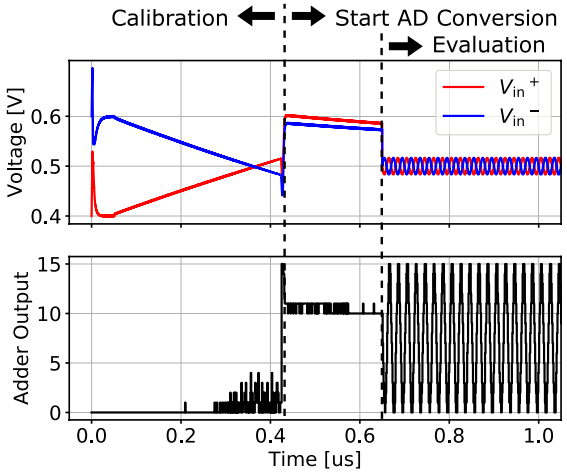


**Fig. 14** Simulated waveform when input frequency is 50 MHz.

ADC achieves the FoM of 93 fJ/conv at Nyquist frequency, where FoM is defined as $P/(2^{\text{ENOB}} \cdot f_{\text{s}})$.

The performance summary and comparisons are shown in Table 1. Our ADC achieves much lower power consumption than the stochastic ADC in Ref. [9]. Compared with the stochastic ADC, our ADC limits the number of active comparators. With this decrease of active comparators, the toggle rate of the adder becomes low, which results in lower

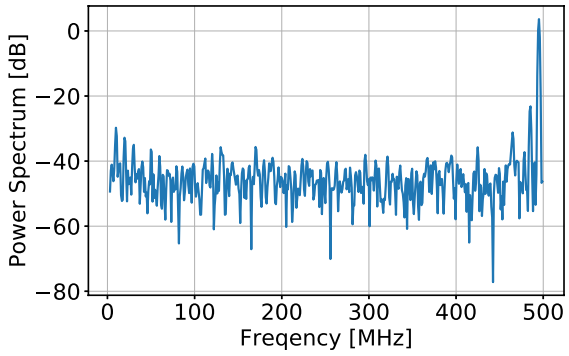


**Fig. 15** Simulated power spectrum when input frequency is near Nyquist frequency.

**Table 1** Performance summary and comparison.

| | This work | [9] | [12] | [13] |
|---|---|---|---|---|
| Technology | 65 nm | 130 nm | 90 nm | 32 nm SOI |
| Architecture | Order based | Stochastic | DAC based | Off-chip Calib. |
| On-chip Selection | Yes | Yes | Yes | No |
| Resolution [bit] | 4 | 5.16 | 4 | 6 |
| Supply Voltage [V] | 1.0 | 1.0 | 1.2 | 0.85 |
| Sampling Rate [GS/s] | 1.0 | 0.32 | 1.5 | 5 |
| Power [mW] | 0.84 | 87 | 23 | 2.5 |
| DNL [LSB] | -0.42/+0.43 | - | - | 0.52 |
| INL [LSB] | -0.46/+0.38 | - | - | 0.37 |
| SNDR@Nyquist [dB] | 20.9 | 32.8 | 24.0 | 30.9 |
| ENOB@Nyquist [bit] | 3.18 | 5.16 | 3.69 | 4.84 |
| FoM [fJ/conv] | 93 | $7.62 \times 10^3$ | $1.47 \times 10^3$ | 59 |

power consumption. The FoM of our ADC architecture is higher than that of Ref. [13]. However, our method implements comparator selection fully on-chip, whereas off-chip measurement is used in Ref. [13].

## 6. Conclusion

In this paper, we proposed a flash ADC architecture that utilizes offset voltage variation by selecting comparators based on the ranking of the offset voltage. We can obtain equally spaced voltage references by selecting appropriate comparators. Our proposed time-domain evaluation of offset voltages enables compact and mostly digital on-chip implementation. We evaluated our proposed 4-bit ADC based on HSPICE simulation using transistor models of a commercial 65-nm process. In the case of using 127 comparators, INLs of 20 simulated chips are in the range of −0.34 LSB/+0.29 LSB to −0.83 LSB/+0.74 LSB, and DNLs are in the range of −0.33 LSB/+0.24 LSB to −0.77 LSB/+1.18 LSB. In addition, from the noise transient simulation, we found that the ADC achieves an SNDR of 20.9 dB at Nyquist-frequency input and the power consumption of 0.84 mW, which results in the FoM of 93 fJ/conv. Since the power consumption of an adder decrease in deeper submicron processes, the same linearity can be expected with less power consumption. In this paper, we demonstrated an application of order statistics to a reference-less ADC topology and confirmed the feasibility of the order statistics based circuit design. Order statistics based approaches may enable new circuit techniques in other applications too.

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