

An 11-nW CMOS Temperature-to-Digital Converter Utilizing Sub-Threshold Current at Sub-Thermal Drain Voltage

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Abstract—A fully integrated CMOS temperature-to-digital converter utilizing MOSFETs in the sub-threshold region is proposed. The temperature-to-digital converter achieves the ultra-low power operation required for Internet of Things (IoT) nodes. The proposed principle takes the ratio of the sub-threshold currents of two nMOSFETs whose drain voltages are maintained well above and well below the thermal voltage, respectively. The proposed circuit implementation of the temperature-to-digital converter achieves ultra-low power consumption of 11 nW at room temperature of 25 °C. Measurement results of the proposed temperature sensor fabricated in a 180-nm CMOS process show $-0.9/+1.2$ °C peak-to-peak inaccuracy over a temperature range of -20 °C to 80 °C after a two-point calibration while achieving a resolution of 145 mK.

Index Terms—Internet of Things (IoT), low power, sub-thermal drain voltage (STV), temperature sensor, temperature-to-digital converter.

I. INTRODUCTION

CMOS-COMPATIBLE smart temperature sensors that can be integrated into a system-on-chip (SoC) have become of great value because of their low cost and ease of use. Applications such as the thermal management of processors or SoCs [1]–[3], ambient temperature monitoring [4], and biomedical devices [5]–[7] are some examples. Recently, with the emergence of the Internet of Things (IoT), the need for sensors with as low-power consumption as possible to extend the battery life has become a focus of research. The low power operation is also required in an IoT node with a battery that has a large internal resistance R_{BAT} . The maximum instantaneous current from a battery (I_{MAX}) is limited owing to the voltage drop caused by the internal resistance R_{BAT} . In the case of a

miniature size IoT node with a solid-state bare die battery [8], I_{MAX} is limited to only 1.7 μ A after 1000 cycles owing to the increased R_{BAT} when the acceptable voltage drop is 100 mV. Therefore, reducing the average current of a temperature sensor to less than 1% of I_{MAX} ($= 17$ nA) is desirable for an IoT node with the battery [8]. Another desirable feature of the temperature sensor for IoT nodes is proportional-to-absolute-temperature (PTAT) output with a digital interface. PTAT output is beneficial for realizing low-power, real-time thermal management because complicated off-chip processing is not required.

This paper describes a fully integrated CMOS temperature-to-digital converter with power consumption of only 11 nW. This paper is an extension of a previous conference paper [9]. The key extensions of this paper over [9] are: 1) a detailed description of the operating principle; 2) a detailed analysis of the error sources; and 3) new chip design and fabrication including digital interface circuits.

The key techniques in our proposed temperature-to-digital converter are as follows: 1) a new temperature-sensing principle that utilizes a sub-threshold current at a sub-thermal drain voltage (STV) and 2) a circuit implementation of the proposed principle in a 180-nm CMOS process which enables the temperature sensor to achieve ultra-low power consumption of 11 nW at 25 °C. The measured resolution is 145 mK, and the measured inaccuracy is $-0.9/+1.2$ °C for nine samples in a temperature range of -20 °C to 80 °C.

The remainder of this paper is organized as follows. Section II reviews the state-of-the-art of temperature sensors. Section III introduces the operation principle of the proposed temperature-sensing mechanism. Section IV proposes an ultra-low-power circuit implementation of the proposed temperature-to-digital converter. Section V demonstrates some measurement results of our temperature-to-digital converter. Section VI concludes this paper.

II. STATE-OF-THE-ART TEMPERATURE SENSORS

An on-chip temperature-to-digital converter that consists of a temperature sensor, its bias circuitry, and an ADC, all integrated into the same die, is often called a smart temperature sensor. For temperature sensing in a CMOS process, the device of choice is a parasitic bipolar junction transistor (BJT), which can be realized using the same diffusions as those used

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for MOSFETs. A BJT-based temperature sensor is generally self-referenced because a self-generated bandgap voltage is used to digitize the base-to-emitter voltage (V_{BE}) difference between two BJTs biased by different collector currents. The voltage difference, ΔV_{BE} , is PTAT thus providing an on-chip digital representation of temperature with the use of an ADC. These sensors are also called bandgap temperature sensors and provide accuracy of less than $\pm 0.1^\circ\text{C}$ under the temperature range of -55°C to 125°C with one-point calibration [10], [11]. One disadvantage of bandgap temperature sensors is that they require high-accuracy ADC circuits to achieve an accurate temperature sensing, which increases their power consumption [12].

To realize a sub-1-V temperature sensor, the replacement of BJTs with diode-connected MOSFETs was proposed in [13]. With the help of a zoom ADC, temperature inaccuracy of $\pm 0.4^\circ\text{C}$ was achieved after one-point calibration with a power consumption of approximately 600 nW (excluding the digital backend). Temperature-sensing mechanisms using the logic gate delay of CMOS have also been proposed, facilitating ease-of-design [14]. Such sensors require calibration with two or three points and also require a nonlinear master curve. Thus, the generation of an on-chip digital output requires further processing that consumes power.

MOSFET sub-threshold current can also be used as a replacement of BJTs to achieve temperature sensing. Sub-threshold MOSFET-based temperature sensors enable a low voltage and low power consumption. Although they suffer from lower accuracy and typically require a two-point calibration, they are expected to be beneficial for many practical applications where the need for high accuracy and resolution can be relaxed. Recently, a new class of temperature sensors utilizing MOSFET sub-threshold current has been proposed. A current-to-frequency converter (CFC)-based temperature sensor, where the frequency of an oscillator becomes exponential to the absolute temperature, was proposed in [12]. To obtain a PTAT digital value, the logarithm operation is required. Furthermore, nonlinear fitting is used to achieve an accuracy of $-0.76/+0.76^\circ\text{C}$. In [15], a 113-pW temperature-to-digital converter with a temperature range of only -20°C to 40°C , which is too limited for many applications, was proposed. Although a 120-nW temperature sensor was also proposed in [16], the covered temperature range was only -10°C – 30°C , and the topology requires an external reference clock, which increases the additional power consumed by its generation. To realize an inherent on-chip PTAT quantity, in [17], a linear approximation of the exponential function, $\exp(x)$, was utilized by choosing the x carefully. The required x was realized by taking the ratio of the sub-threshold currents of two MOSFETs biased at different V_{GS} values. The linearity of the sensor was dependent on the optimum value, which may vary because of mismatch.

In this paper, we take a similar approach to that used in [17] but use a different physical phenomenon to obtain the PTAT quantity. We keep the V_{GS} value the same but apply different V_{DS} values to the two MOSFETs. By setting the V_{DS} for one MOSFET much larger than the thermal voltage V_T and setting V_{DS} for the other MOSFET below V_T , the corresponding

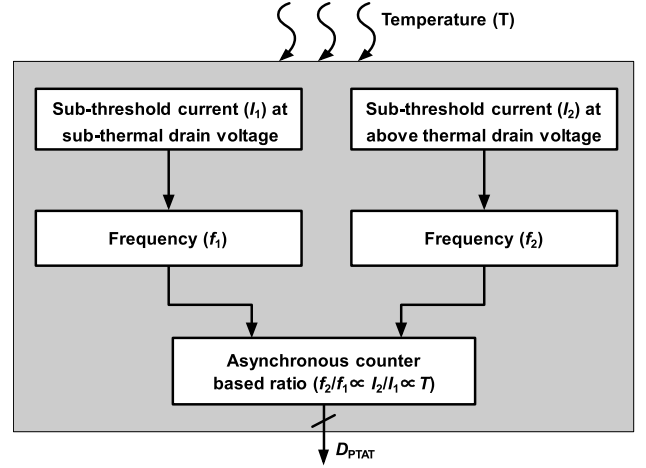


Fig. 1. Flowchart of the proposed temperature-to-digital converter.

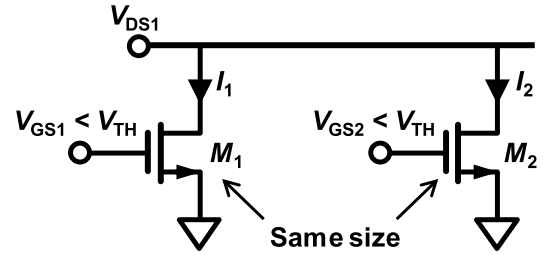


Fig. 2. Mechanism of the conventional temperature sensing [17].

current ratio provides better linearity and sensitivity than those obtained by the mechanism proposed in [17].

III. PROPOSED TEMPERATURE-SENSING MECHANISM

Fig. 1 shows a flowchart of the proposed temperature-to-digital converter. The process of conversion from the temperature to a PTAT digital output has three steps: 1) generation of two sub-threshold currents obtained from a pair of nMOSFETs with different drain voltages (I_1 , I_2); 2) current-to-frequency conversion (f_1 , f_2); and 3) frequency ratio (f_2/f_1) calculation for the PTAT digital output (D_{PTAT}). The key point here is that the current ratio I_2/I_1 shows a PTAT characteristic in the target temperature range of -20°C to 80°C . The details of the principle of achieving a PTAT I_2/I_1 are described in the next.

A. Temperature Sensing Mechanism

A PTAT I_2/I_1 is required to realize the proposed temperature-to-digital converter shown in Fig. 1. Fig. 2 shows the temperature-sensing principle of a conventional work [17] that achieves a PTAT I_2/I_1 by approximating an exponential function by a linear function. In [17], two identical nMOSFETs in the sub-threshold region with different gate voltages of V_{GS1} and V_{GS2} were implemented to achieve a PTAT I_2/I_1 . The current ratio of I_2 to I_1 is expressed as

$$\frac{I_2}{I_1} = \exp\left(\frac{\Delta V_{GS}}{nV_T}\right) \quad (1)$$

where $\Delta V_{GS} = V_{GS2} - V_{GS1}$, $V_T (= kT/q)$ is the thermal voltage, k is Boltzmann's constant, q is the electron charge, T is the absolute temperature, and n is the sub-threshold swing

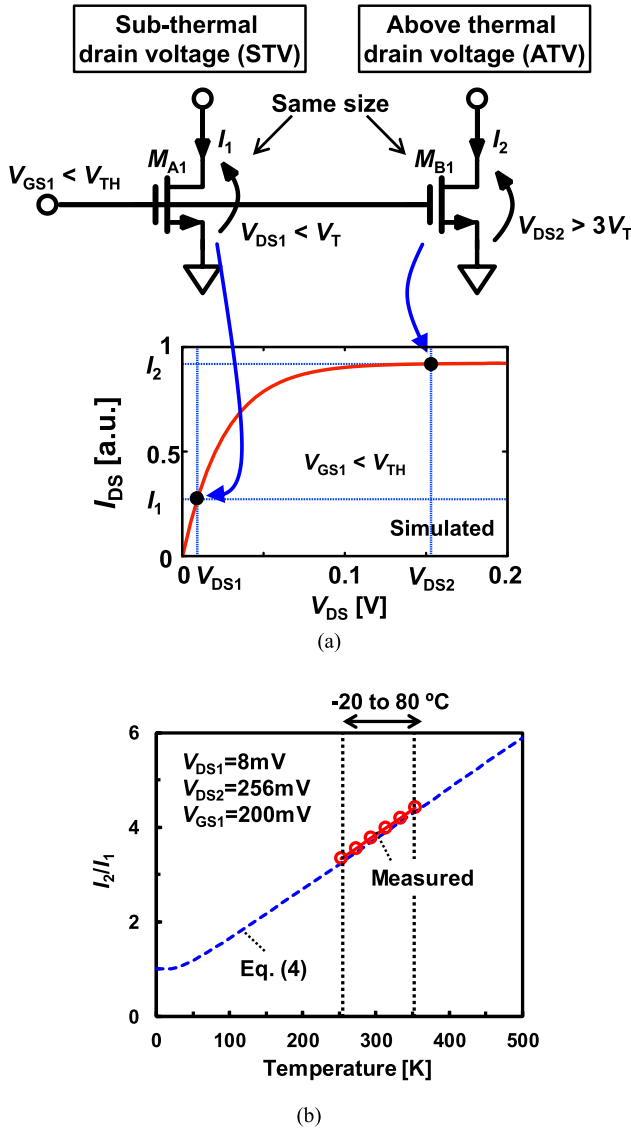


Fig. 3. Proposed temperature-sensing mechanism. (a) V_{DS} biasing of MOSFETs. (b) Theoretical and measured I_2/I_1 for a single transistor.

parameter. In (1), I_2/I_1 has an optimum ΔV_{GS} that maximizes the linearity of I_2/I_1 in a temperature range. For a typical n of 1.4, the optimum ΔV_{GS} is -72 mV in the temperature range of -20 °C to 80 °C. The sensitivity of I_2/I_1 is calculated to be $0.0009/^\circ\text{C}$ when ΔV_{GS} is -72 mV.

Fig. 3(a) shows the operating principle of our proposed temperature-sensing mechanism. Two identical nMOSFETs M_{A1} and M_{B1} operating in the sub-threshold region are biased with different V_{DS} values. An STV less than the thermal voltage $V_T (= 26$ mV at 27 °C) is applied to V_{DS1} , while above thermal drain voltage (ATV) more than $3 V_T$ is applied to V_{DS2} . As a result, drain currents of M_{A1} and M_{B1} are expressed as follows [18]:

$$I_1 = K \cdot \exp\left(\frac{V_{GS1} - V_{TH}}{n V_T}\right) \cdot \left(1 - \exp\left(\frac{-V_{DS1}}{V_T}\right)\right) \quad (2)$$

$$I_2 = K \cdot \exp\left(\frac{V_{GS1} - V_{TH}}{n V_T}\right) \quad (3)$$

where K is a technology-related parameter and V_{TH} is the threshold voltage of the transistors. The current ratio I_2/I_1

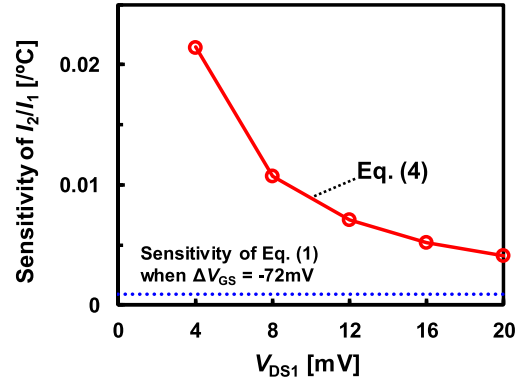


Fig. 4. Sensitivity of I_2/I_1 .

becomes a function of V_{DS1} and T as follows:

$$\frac{I_2}{I_1} = \frac{1}{1 - \exp\left(\frac{-V_{DS1}}{V_T}\right)}. \quad (4)$$

Assuming that V_{DS1} is sufficiently smaller than V_T , I_2/I_1 is approximated as

$$\frac{I_2}{I_1} = \frac{V_T}{V_{DS1}} + C \quad (5)$$

where C is a temperature-independent constant. Equation (5) shows that the sensitivity of I_2/I_1 to T can be improved by reducing V_{DS1} . I_2/I_1 in (4) with V_{DS1} of 8 mV is plotted in Fig. 3(b) along with the measured I_2/I_1 in the temperature range of -20 °C to 80 °C using a single nMOSFET implemented in a 180 -nm CMOS process. The theoretical slope (= sensitivity) of I_2/I_1 obtained from (5) is $0.0107/^\circ\text{C}$, whereas the measured slope of I_2/I_1 is $0.0108/^\circ\text{C}$. The measured and theoretical slopes agree within an error of 1% . Fig. 4 shows the theoretical sensitivity of I_2/I_1 obtained from (5). The proposed principle has over ten times higher sensitivity than that in [17] when ΔV_{GS} in (1) is set to -72 mV and V_{DS1} in (5) is set to 8 mV. Fig. 5(a) shows the adjusted R^2 for (4) versus V_{DS1} in the temperature range of -20 °C to 80 °C with the adjusted R^2 in (1) obtained when $\Delta V_{GS} = -72$ mV. Theoretically, the proposed temperature sensing mechanism shows higher linearity when $V_{DS1} < 12$ mV. Fig. 5(b) shows the peak-to-peak inaccuracy of I_2/I_1 in the temperature range of -20 °C to 80 °C. Two-point calibration is performed by reading I_2/I_1 at 0 °C and 60 °C. The proposed temperature sensing mechanism enables both higher sensitivity and better linearity than those in [17].

B. Mismatch Effect

The matching of M_{A1} and M_{B1} is important in the proposed temperature sensing principle. A mismatch between M_{A1} and M_{B1} may affect the linearity of I_2/I_1 . Considering the mismatch between M_{A1} and M_{B1} , (4) is modified to

$$\begin{aligned} \frac{I_2}{I_1} &= \exp\left(\frac{-\Delta V_{TH}}{n V_T}\right) \frac{1}{1 - \exp\left(\frac{-V_{DS1}}{V_T}\right)} \\ &= K_0(T) \frac{1}{1 - \exp\left(\frac{-V_{DS1}}{V_T}\right)} \end{aligned} \quad (6)$$

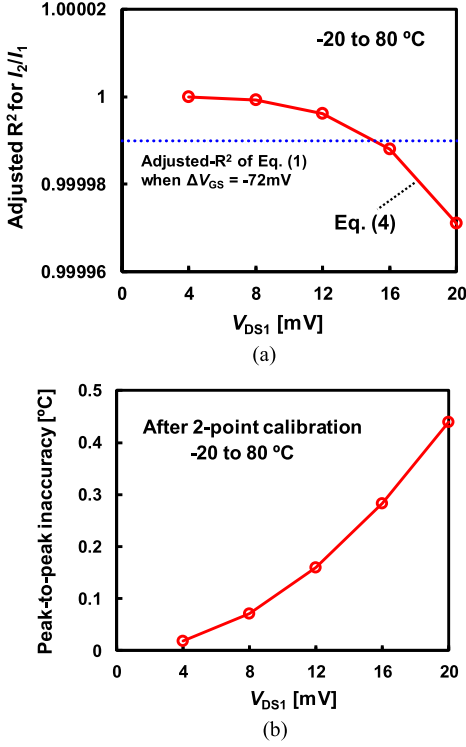


Fig. 5. (a) Adjusted R^2 of I_2/I_1 . (b) Inaccuracy of the temperature-sensing calculated from I_2/I_1 .

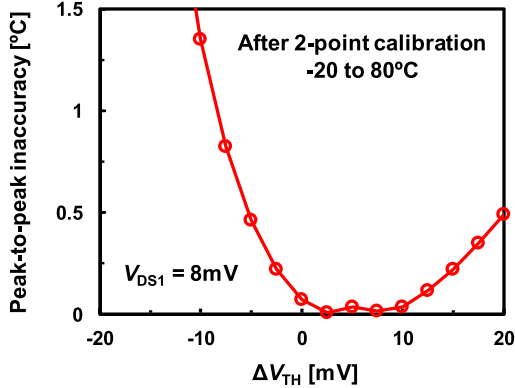


Fig. 6. Effect of the transistor mismatch on the accuracy of the temperature sensing.

where $\Delta V_{TH} = V_{TH2} - V_{TH1}$. When $\Delta V_{TH} \ll nV_T$, $K_0(T)$ is approximated as 1 and I_2/I_1 shows the PTAT characteristics in (5). Conversely, when ΔV_{TH} is not sufficiently smaller than nV_T , the accuracy of I_2/I_1 is affected by the mismatch. Fig. 6 shows the ΔV_{TH} dependence of the inaccuracy of I_2/I_1 after a two-point calibration obtained from (6) in the temperature range of -20 °C to 80 °C. n of 1.4 obtained from a SPICE simulation was used for the analysis. The error of 0.07 °C at $\Delta V_{TH} = 0$ is the inherent inaccuracy of I_2/I_1 when V_{DS1} is set to 8 mV as shown in Fig. 5(b). These results show that the mismatch of the transistor pair may reduce the accuracy of I_2/I_1 .

ΔV_{TH} for a pair of MOSFETs is described by the standard deviation

$$\sigma_{\Delta V_{TH}} = \frac{A_{VT}}{\sqrt{WL}} \quad (7)$$

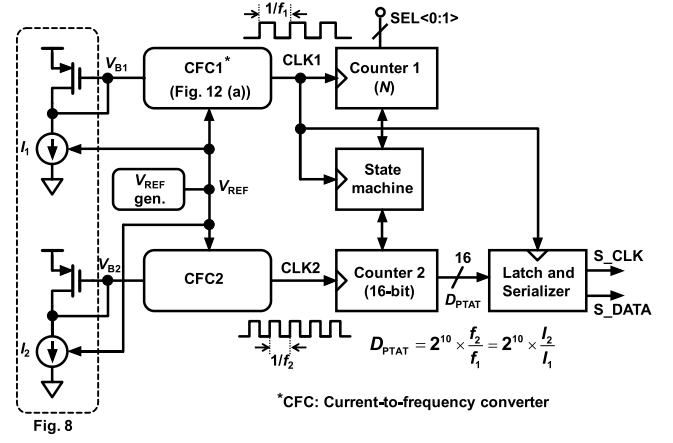


Fig. 7. Overall block diagram of the proposed temperature-to-digital converter.

where A_{VT} is the slope in Pelgrom plot [19]. Using a typical A_{VT} of 3.3 mV· μ m for a 180-nm CMOS process [20], we set W and L for the transistors as 8.0 and 1.5 μ m, respectively, which give $\sigma_{\Delta V_{TH}}$ of 0.95 mV. Thus, according to Fig. 6, an additional peak-to-peak error of 0.3 °C may occur considering the $3\sigma_{\Delta V_{TH}}$ value of the ΔV_{TH} mismatch.

IV. DESIGN OF TEMPERATURE-TO-DIGITAL CONVERTER

Fig. 7 shows a block diagram of the proposed temperature-to-digital converter. The current generators generate currents I_1 and I_2 obtained from nMOSFETs with different drain voltages. Two clock signals, CLK1 and CLK2, are generated using CFCs based on relaxation oscillators. The corresponding frequencies f_1 and f_2 are linear to the currents I_1 and I_2 , respectively. As a result, f_2/f_1 shows the same PTAT characteristic as I_2/I_1 . The counter-based scheme in [21] is used to readout the PTAT digital output. CLK1 and CLK2 are fed to two asynchronous binary counters that enable the on-chip digital conversion of f_2/f_1 ($= I_2/I_1$) without any external clock references. CLK2 edge is counted until CLK1 edge has been counted up to a predefined number N . When CLK1 has been counted to N , the value of Counter 2 ($= D_{PTAT}$) is latched and converted to a 16-bit serial output (S_DATA). In our design, N can be programed in the range of 10–13 bits. The programmability of N enables the programing of the resolution of the temperature-to-digital converter. The resolution has a tradeoff relationship with the conversion time, i.e., m times finer resolution requires m times larger conversion time. Designers or users should select the highest resolution while meeting the required conversion time in the usage. In our temperature-to-digital converter, a voltage reference is implemented to supply a constant voltage V_{REF} for the analog components. The voltage reference makes the temperature-to-digital converter free from external references. In our design, a two-transistor-based on-chip voltage reference presented in [22] is used.

A. Current Generators

In the proposed principle shown in Fig. 3(a), a circuit implementation that regulates V_{DS1} to an STV and V_{DS2} to an ATV is required. In particular, a temperature-independent

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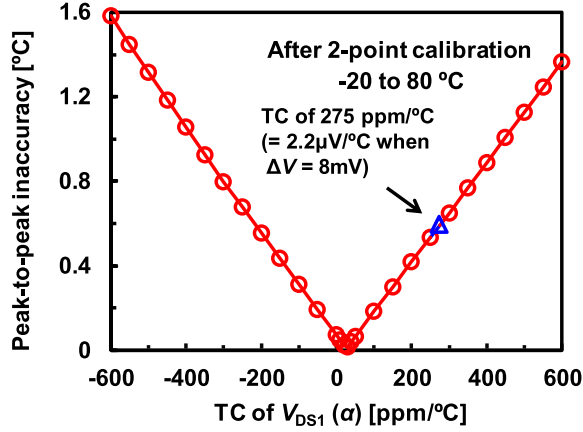


Fig. 10. Dependence of the inaccuracy of the temperature sensing on the temperature coefficient of V_{DS1} when the target $V_{DS1} = 8$ mV.

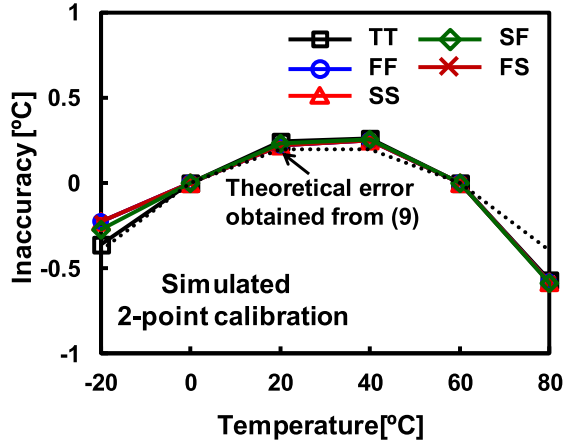


Fig. 11. Process corner analysis of the inaccuracy of the temperature sensing.

where M is the number of diodes in the voltage divider, V_{REF}/M ($= \Delta V$) is the target V_{DS1} , and T_R is a reference temperature, I_2/I_1 is given as

$$\frac{I_2}{I_1} = \frac{1}{1 - \exp\left(-\Delta V \frac{1 + \alpha(T - T_R) \times 10^{-6}}{V_T}\right)}. \quad (9)$$

Fig. 10 shows the peak-to-peak temperature errors using I_2/I_1 in (9) after two-point calibration when $T_R = -20$ °C, and the target temperature range is -20 °C to 80 °C. As shown in Fig. 10, an increase in the temperature dependence of V_{DS1} increases the error. In our design, $k = 16$ is selected, resulting in $\alpha = 2.2$ $\mu\text{V}/^\circ\text{C}$ and, in theory, to a 0.6 °C inaccuracy in I_2/I_1 when $\Delta V = 8$ mV. Fig. 11 shows the simulated inaccuracy of I_2/I_1 for our designed current generators for different process corners. The worst simulated peak-to-peak inaccuracy is 0.84 °C in the process corners. The obtained simulated results relatively differ from the theoretical error obtained from (9) at high temperatures. One possible reason is that the theoretical error shown in (9) is introduced under the condition that the TC of V_{DS1} is first order. If we can include higher order factors, the model will be improved to match the actual characteristics. The accuracy of I_2/I_1 can be further improved by increasing k at the cost of the

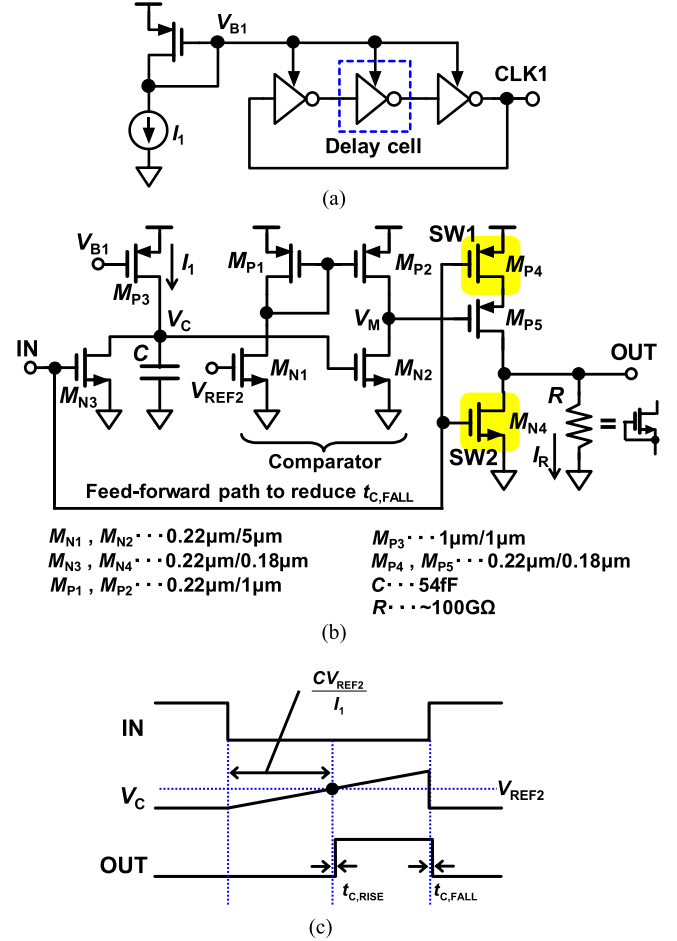


Fig. 12. (a) Concept of the CFC. (b) Schematic of the delay cell. (c) Timing diagram of the delay cell.

increased area. Thus, the proposed technique achieves a constant V_{DS1} and V_{DS2} with a small current overhead of 350 pA.

B. Current-to-Frequency Converter

In Fig. 7, the oscillation frequency of CLK1 (CLK2) must be highly linear to I_1 (I_2). The proposed CFCs are based on a relaxation oscillator as shown in Fig. 12(a). The oscillation period of CFC1 is expressed as

$$T_{OSC,1} = N_{CELL} \left(\frac{C V_{REF2}}{I_1} + t_{C,FALL} + t_{C,RISE} \right) \quad (10)$$

where N_{CELL} ($= 3$ in our design) is the number of delay cells in CFC1, and $t_{C,FALL}$ and $t_{C,RISE}$ are the propagation delays of the proposed delay cell in the CFCs. V_{REF2} is a fixed voltage for the comparators in the delay cells obtained from the diode chain in Fig. 8. The oscillation period of CFC2 ($= T_{OSC,2}$) is also obtained from (10) by exchanging I_1 with I_2 . $t_{C,FALL}$ and $t_{C,RISE}$ should be sufficiently small compared with $C V_{REF2}/I_1$ so that $T_{OSC,1}$ becomes proportional to $C V_{REF2}/I_1$. In this case, f_2/f_1 ($= T_{OSC,1}/T_{OSC,2}$) gives the same PTAT characteristics as I_2/I_1 . In the delay cell shown in Fig. 12(b), the first stage is a differential amplifier with a pMOSFET current mirror load acting as a comparator. The negative input is biased at V_{REF2} ($< V_{TH}$). In the second stage, a common-source amplifier with a large load resistor is implemented to reduce $t_{C,RISE}$.

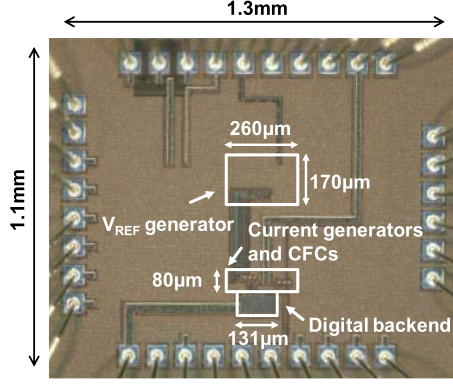


Fig. 13. Chip photograph of the proposed temperature-to-digital converter.

The load resistor is implemented with an OFF transistor. To achieve sub-1-nW static power consumption in the delay cell, the resistor (R) should be large (e.g., 5 G Ω). However, the large R increases $t_{C,FALL}$ owing to the limited current I_R . To reduce $t_{C,FALL}$, we utilize a split-output scheme [23] that decouples the comparator stage from the pull-down path. A feed-forward path composed of SW1 and SW2 is added in the second stage in Fig. 12(b). When IN changes from low to high, the propagation through the first stage and the second stage in the comparator is bypassed and OUT is pulled down by SW2, which leads to the reduction of $t_{C,FALL}$. In the simulation, $t_{C,RISE}$ and $t_{C,FALL}$ are reduced to less than 2% and 0.1% of CV_{REF}/I_1 , respectively, in the temperature range of -20°C to 80°C at $V_{DD} = 0.8\text{ V}$.

The frequencies of the CFCs are set to over 1 kHz to make the conversion within 1 s at room temperature when $N = 10$ bits in Fig. 6. The frequencies of CFCs are temperature dependent that makes the conversion time of the temperature sensor temperature-dependent. In our measurement, f_1 ranged from 100 Hz to 10 kHz in the temperature range of -20°C to 80°C . If the temperature sensor is used in the wide temperature range especially in lower than 0°C , designers must consider that the temperature sensor meets the demand for conversion time. The conversion time can be improved at the cost of the power consumption or resolution by reducing N in Fig. 7.

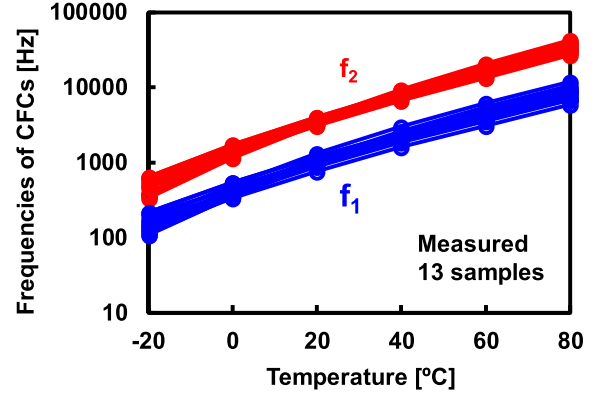
C. Voltage Reference

In the temperature sensor, a voltage reference is required to achieve the current generators shown in Fig. 8. In this paper, two-transistor-based voltage reference presented in [22] is applied to the current generators which operate with nW power consumption. On the other hand, a standard voltage V_{REF} supplied by two-transistor voltage reference has temperature dependence due to the mismatch [24]. We assume that V_{REF} with a temperature coefficient β ppm/ $^\circ\text{C}$ is given by

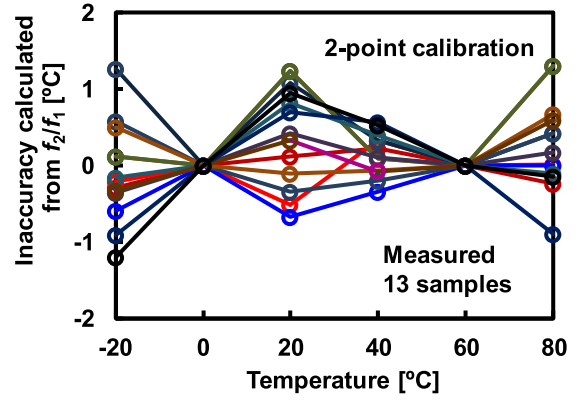
$$V_{REF} = V_{REF,R} + \beta V_{REF,R}(T - T_R) \times 10^{-6} \quad (11)$$

where $V_{REF,R}$ is V_{REF} when T is a reference temperature T_R . By substituting (11) into (8), V_{DS1} is expressed as

$$V_{DS1} \approx \frac{V_{REF,R}}{M} (1 + (\alpha + \beta)(T - T_R) \times 10^{-6}). \quad (12)$$



(a)



(b)

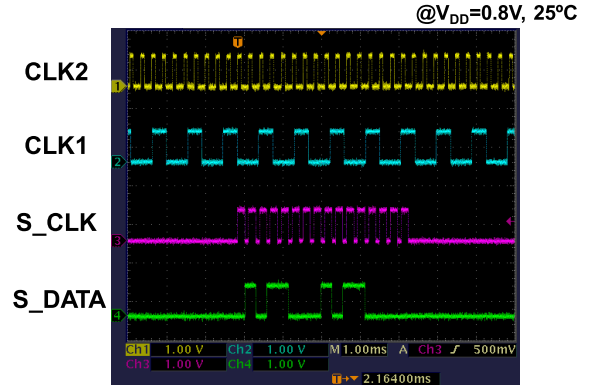
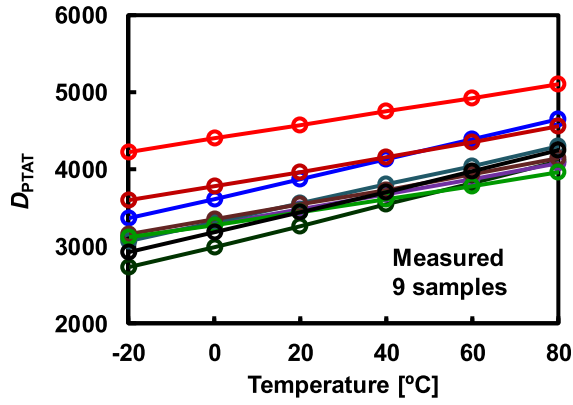
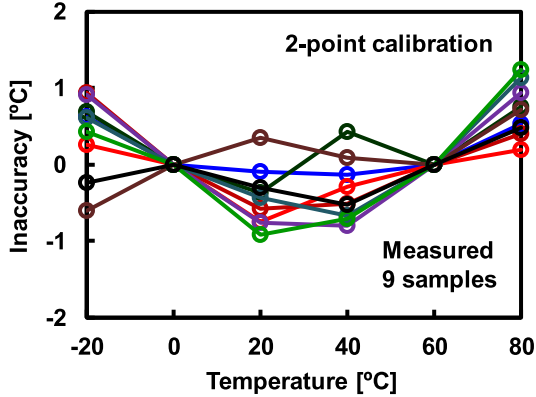
Fig. 14. (a) Frequencies of the CFCs. (b) Inaccuracy of the temperature sensors calculated from f_2/f_1 [9].

Fig. 15. Measured waveforms of the proposed temperature-to-digital converter.

The peak-to-peak temperature inaccuracy obtained from I_2/I_1 , under the condition that V_{REF} has a TC of β , $T_R = -20^\circ\text{C}$, and $V_{REF,R}/M = 8\text{ mV}$, can then be estimated from Fig. 10 by replacing α with $\alpha + \beta$. Overall, temperature affects V_{DS1} in two ways. The first effect comes from the V_{REF} itself. The second effect comes from the current generators as shown in Fig. 9. Thus, the TC variability of V_{DS1} is a statistical sum of TCs of ΔV and the current generator as shown in (12). The reported absolute TC of a two-transistor voltage reference [24] without trimming is ranged from 17 to 231 ppm/ $^\circ\text{C}$. In the worst case, i.e., when V_{REF} has a TC of 231 ppm/ $^\circ\text{C}$, the peak-to-peak inaccuracy of I_2/I_1 is 1.2 $^\circ\text{C}$ in our simulation.



(a)



(b)

Fig. 16. Measured (a) D_{PTAT} and (b) temperature inaccuracy among nine dies.

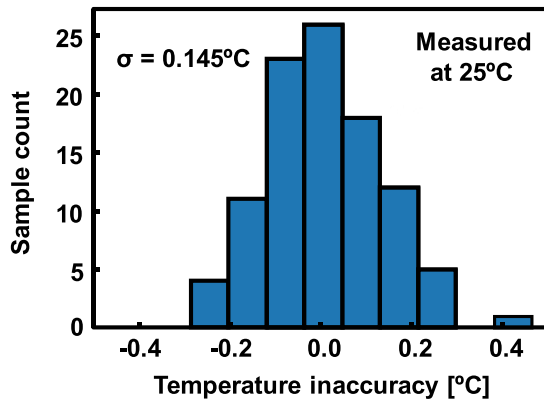


Fig. 17. Measured temperature inaccuracy of 100 reading.

Post-fabrication one-temperature point trimming is an effective method of reducing the TC of V_{REF} [24]. In [24], the 2T voltage reference utilizing the trimming method reduces the worst TC of V_{REF} to less than 47 ppm/°C, which reduces the simulated peak-to-peak inaccuracy of the proposed temperature sensing to less than 0.9 °C. By implementing trimming for the voltage reference, the accuracy of the temperature sensor can be improved.

V. MEASUREMENT RESULTS

The proposed temperature-to-digital converter including a voltage reference [22] and digital backend is fabricated in a 180-nm CMOS process.

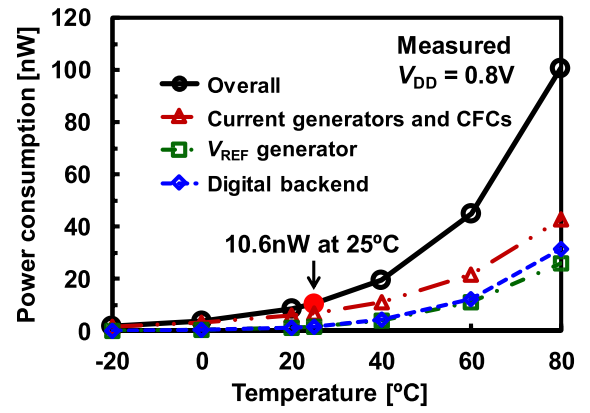


Fig. 18. Power consumption of the temperature-to-digital converter.

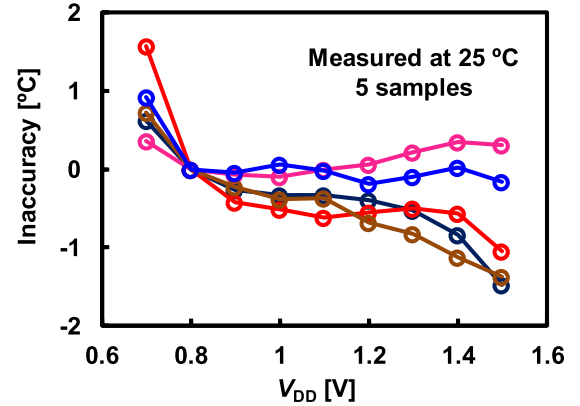


Fig. 19. V_{DD} dependence of the temperature inaccuracy.

Fig. 13 shows a chip photograph of our temperature-to-digital converter. The total area of the temperature-to-digital converter including the digital backend is 0.074 mm². In [9], to measure the inaccuracy of the temperature sensor, f_1 and f_2 were measured with an oscilloscope as shown in Fig. 14(a), and the inaccuracy was estimated by taking f_2/f_1 as shown in Fig. 14(b). In this paper, the digital serialized D_{PTAT} (= S_DATA in Fig. 7) is read for the samples to measure the accuracy and resolution of the temperature sensor. Fig. 15 shows the waveforms of CLK1, CLK2, S_CLK, and S_DATA shown in Fig. 7 at 0.8 V and 25 °C. Fig. 16(a) shows the obtained D_{PTAT} of nine samples in the temperature range of −20 °C to 80 °C, while Fig. 16(b) shows the inaccuracy of the temperature-to-digital converters. After a two-point calibration, the peak-to-peak inaccuracy of the nine samples in this paper is −0.9/+1.2 °C. The counter-resolution, which is the LSB associated with the 10-bit conversion of the temperature-to-digital converter, among the measured samples is 94 mK. Owing to the thermal noise, the sampled counter value D_{PTAT} varies in each measurement. To evaluate the sensory resolution, D_{PTAT} is measured 100 times at a fixed temperature (25 °C in this paper) [25]. Fig. 17 shows the 100 samples of the temperature inaccuracy. The standard deviation of the samples is 1.54 LSB, which corresponds to a noise-limited resolution of 145 mK. Fig. 18 shows the power consumption of the entire circuit and each component in the temperature-to-digital converter. The power consumption of the entire circuit is 10.6 nW at room temperature (25 °C).

TABLE I
COMPARISON WITH PREVIOUSLY PUBLISHED MOSFET-BASED LOW-POWER TEMPERATURE SENSORS

	This work (w/ digital backend)	CICC'19 (w/o digital backend)	JSSC'14 [21]	A-SSCC'14 [17]	ISSCC'17 [12]	ISSCC'14 [13]
CMOS process [nm]	180	180	180	65	180	160
PTAT digital output	Yes	Yes	Yes	Yes	No	Yes
Type	MOSFET	MOSFET	MOSFET	MOSFET	MOSFET	DTMOS
Area [mm ²]	0.074	0.065	0.09	0.022	0.22	0.085
Supply voltage	0.8	0.8	1.2	0.4	1.2	0.85
Power [nW]	11	13 ^{*1}	71	280	570	600
Conversion time [ms]	839 (at 25°C)	861 (at 25°C)	30	25	8	6
Energy/conversion [nJ]	8.9	11	2.2	7	4.6	3.6
Temperature range [°C]	-20 ~ 80	-20 ~ 80	0 ~ 100	0 ~ 100	-20 ~ 80	-40 ~ 125
Inaccuracy [°C]	-0.9/1.2 ^{*2} (9 samples)	-1.2/1.3 ^{*2} (13 samples)	-1.4/1.5 ^{*2} (18 samples)	-1.6/1.0 ^{*2} (8 samples)	-0.76/0.76 ^{*3} (5 samples)	-0.4/0.4 ^{*3} (16 samples)
Calibration point	2-point	2-point	2-point	2-point	2-point	1-point
Resolution [mK]	94 ^{*4} 145 ^{*5}	105 ^{*4}	300 ^{*5}	250 ^{*6}	90 ^{*5}	63 ^{*5}
Resolution FoM ^{*7} [nJ·K ²]	0.19	0.14 ^{*8}	0.19	0.44	0.037	0.0141
V _{DD} sensitivity [°C/V]	3.8 at 25°C, 0.7 ~ 1.5 V (5 samples)	4.6 at 20°C, 0.8 ~ 1.4 V (3 samples)	14 at 25°C, 1.0 ~ 1.4 V (1 sample)	N/A	0.36, 0.8 ~ 1.8 V	0.45, 0.85 ~ 1.2 V

*1) Power consumption of digital backend is estimated by simulation

*2) Peak-to-peak inaccuracy

*3) 3 σ inaccuracy

*4) Counter resolution

*5) Noise-limited resolution

*6) Definition of resolution is not clearly mentioned

*7) Resolution FoM = (Energy/Conversion) \times (Resolution)² [26]

*8) Calculated from counter resolution

The current generators and CFCs consume 6.9 nW, V_{REF} generator and digital backend consume 1.9 and 1.8 nW, respectively. The power consumption of the voltage reference is increased from that of [9] so that it is less affected by the switching noise from the digital circuits. Even when the temperature increases to 80 °C, the power consumption of the entire circuit is 100 nW. Fig. 19 shows the measured V_{DD} dependence of temperature inaccuracy for five samples at 25 °C. The inaccuracy over a V_{DD} range from 0.7–1.5 V is $-1.5/+1.6$ °C which results in a V_{DD} sensitivity of 3.8 °C/V.

In Table I, the performance of the proposed temperature-to-digital converter and the previous MOSFET-based low-power temperature sensors are summarized and compared. The proposed temperature-to-digital converter has the lowest power consumption of 11 nW at 25 °C in Table I, while achieving a competitive inaccuracy of $-0.9/+1.2$ °C among nine samples and a resolution of 145 mK.

VI. CONCLUSION

In this paper, an 11-nW ultra-low power temperature-to-digital converter is proposed. A new principle of the temperature sensing based on the sub-threshold operation at STV contributes to realizing a linear PTAT digital output while achieving a competitive resolution. A circuit implementation of the current generators and CFCs realizes the proposed sensing principle under the ultra-low power operation. The circuit implementation of the temperature-to-digital converter achieves the lowest power consumption of 11 nW among the temperature sensors that covers the temperature range of -20 °C to 80 °C. Measurement results of the test

chips fabricated in a 180-nm CMOS process show that the temperature-to-digital converter realizes $-0.9/+1.2$ °C inaccuracy over a temperature range of -20 °C to 80 °C with a resolution of 145 mK.

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