A Statistical Modeling Methodology of RTN Gate Size Dependency Based on Skewed Ring Oscillators

A.K.M. Mahfuzul Islam*, Tatsuya Nakai†, and Hidetoshi Onodera†
* Institute of Industrial Science, The University of Tokyo, 4-6-1 Komaba, Meguro-ku, Tokyo 153-8505, JAPAN.
e-mail: mahfuzul@iis.u-tokyo.ac.jp
Tel: +81-3-5452-6253, Fax: +81-3-552-6632
† Graduate School of Informatics, Kyoto University, Yoshida-honmachi, Sakyo-ku, Kyoto 606-8501, JAPAN.
e-mail: {tnakai,onodera}@vlsi.kuee.kyoto-u.ac.jp
Tel: +81-75-753-5353, Fax: +81-75-753-5343

***Abstract*—This paper proposes a statistical modeling methodology of RTN (Random Telegraph Noise) gate size dependency utilizing skewed ring oscillator (RO) structures. An iterative characterization flow is developed to estimate RTN induced threshold distribution of each gate sizes of pMOSFET and nMOSFET independently. The skewed RO based test structure was fabricated in a 65 nm SOTB (Silicon On Thin Body) process. It is observed that Lognormal distribution represents RTN induced delay distribution well. RTN model of gate size dependency is then developed and validated using the measured data. Model based delay distribution estimation and measurement match well. The proposed extraction methodology is thus suitable for estimating RTN of transistors with arbitrary gate size. The model helps reliability and worst case analysis of digital circuits where transistors of various gate sizes are used.**

I. Introduction

With technology scaling, RTN induced threshold voltage variation ΔV_{T} is becoming significant [1]. There are reports of RTN in SRAMs [2], ring oscillators (RO) [3], and Flash memories [4]. At low voltage operation, frequency fluctuation of 10.4 % has been reported for a 40 nm process [3]. As RTN induced ΔV_{T} distribution has long tails, worst case delay degradation is severe compared with process variation. In a digital circuit, transistors of different gate sizes and lengths are used to optimize delay and power. For design time optimization and reliability analysis, RTN models incorporating channel width and length dependencies are required. In this paper, we focus on RTN modeling of gate size dependency based on delay measurement. We propose a test structure comprised of an array of ring oscillators (RO) with different skewed inverters. We build RTN models for pMOSFET and nMOSFET separately that can be applied to transistor of arbitrary sizes. This eliminates the need to characterize transistor RTN for each of the gate sizes used in a standard cell library.

As RTN is a statistical phenomena and have dynamic nature, measurement and characterization of RTN consumes time. Transistor I–V based characterization is the most common method [5]. However, in a digital circuit environment, the transistors operate under switching conditions. Therefore, an embedded test structure in a digital circuit will provide in-situ RTN properties of switching behavior. For example distribution of total ΔV_{T} amplitude due to complex RTN can differ from convolution of individual trap ΔV_{T} distribution [6]. RO based delay fluctuation measurement can be used to characterize RTN properties under switching conditions [3]. To enable transistor level characterization of RTN using ROs, tuning of the inverter topology [7] or the transistor sizes are performed so that measured delay variation can be related to a particular transistor [8]. This gives us in-situ characterization of transistor RTN under switching conditions. We have proposed such RO structures and their characterization methodology in Refs. [7, 9]. A topology reconfigurable RO structure can be used to further amplify RTN effects of the target transistors [9].

In the RO structures mentioned above, transistor sizing needs to be tuned such that the delay fluctuation can be attributed only to a particular transistor. The required sizing ratio varies depending on the RTN distribution spread. A large spread will require a larger sizing ratio. Another key feature to emulate actual digital circuit behavior is to evaluate multi-stage delay instead of a single stage. A homogeneous structure rather than an inhomogeneous structure is thus more representative of a digital circuit behavior. However, using a homogeneous structure, obtaining transistor level ΔV_{T} distribution is difficult as other transistors in the RO contribute to overall delay fluctuation. In this paper, we propose a new characterization methodology that utilizes the convolution and de-convolution operations to sum or deduct distributions, and show that the methodology can be used to estimate efficient transistor level RTN models using the homogeneous structures.

Our goal is to build RTN models for pMOSFET and nMOSFET separately that incorporates transistor gate size dependency similar to the one used for modeling static ΔV_{T} variation known as the Pelgrom model [10]. We find that the amount of overall fluctuation can be modeled by a Lognormal distribution. As the Lognormal distribution has two parameters, we evaluate their size dependency, and develop a model that can be used to predict RTN for arbitrary size transistor.

We describe our test structure and its design methodology is Sec. II. We then describe our proposed statistical modeling methodology for gate size dependency extraction. We present and discuss the measurement results in Sec. III. We put our concluding remarks in Sec. IV.

978-1-5090-3615-8/17 $31.00 © 2017 IEEE

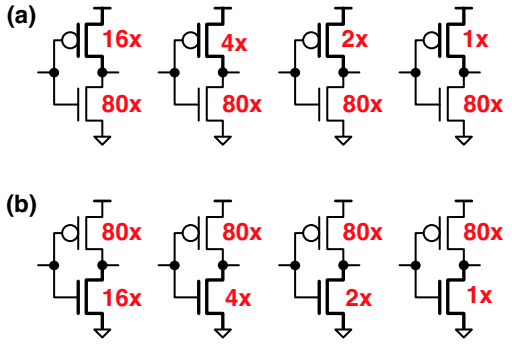


Fig. 1: Concept of skewed inverter design for RTN gate size dependency modeling. (a) pMOSFET dominant, (b) nMOSFET dominant.

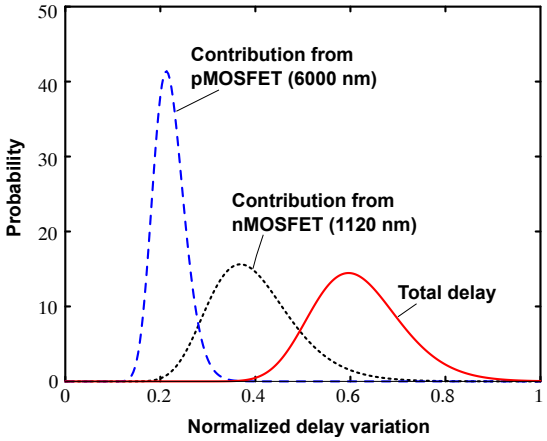


Fig. 2: Contributions of transistors in a RO to total delay distribution. Total delay distribution is the convolution of two delay distributions caused by noises. One distribution is caused by the RTN in the smaller nMOSFET. The other distribution is caused by the larger pMOSFETs.

II. Characterization and Modeling Methodology

A. Test Structure Design Methodology

In this paper, we show that skewed inverters of different ratios can be utilized to build RTN model for gate size dependency. Fig. 1 shows the design methodology of skewed inverters. Two series of skewed inverters are used. In one series, pMOSFET is larger than the nMOSFET and vice versa. The key point here is to keep the larger MOSFET size same and change the smaller transistor size ratios so that a single distribution can be used for the larger transistor across the ROs. If we have a sufficient model to estimate the delay contribution from larger transistors, delay contribution from the smaller transistors can be estimated by de-convolving larger transistor distribution from the total ΔD distribution. Iterating and updating the RTN gate size dependency model will eventually converge to a point where distributions of all ROs are fitted well. We then obtain our final RTN gate sized dependency model.

B. RTN Induced Delay Distribution

In evaluating the total variation, we use the maximum and minimum values and take their differences.

$$\Delta D = D_{\mathrm{MAX}} - D_{\mathrm{MIN}}. \tag{1}$$

In a homogeneous RO structure, all the inverter stages share the same topology. We use skewed inverters in this test structure where we denote ΔV_{T} distribution for the smaller transistor as V_{TARGET}. V_{OTHER} is used to represent distribution for the larger transistor. Multiple RO instances of the same ratio are measured to obtain the distributions. Total delay distribution Z_{MEAS} can be expressed as the sum of distributions contributed by both the smaller and larger transistors as in (4). The delay contributions from each transistor can be modeled by multiplying sensitivity coefficient to ΔV_{T}.

$$X_{\mathrm{TARGET}} = \sum_i k^i_{\mathrm{TARGET}} \cdot V^i_{\mathrm{TARGET}}, \tag{2}$$

$$X_{\mathrm{OTHER}} = \sum_i k^i_{\mathrm{OTHER}} \cdot V^i_{\mathrm{OTHER}}, \tag{3}$$

$$Z_{\mathrm{MEAS}} = X_{\mathrm{TARGET}} + X_{\mathrm{OTHER}}. \tag{4}$$

Here, X_{TARGET} is the delay distribution contributed by the small transistors. X_{OTHER} is the delay distribution contributed by the large transistors. k^i_{TARGET} and k^i_{OTHER} are sensitivity coefficients. V^i_{TARGET} and V^i_{OTHER} represent distributions for the i-th stage transistors. Z_{MEAS} is the measured delay distribution.

Fig. 2 shows simulated probability distribution functions (PDF) of X_{TARGET}, X_{OTHERS} and Z_{MEAS} for a RO where gate sizes of nMOSFET and pMOSFET are 1120 nm and 6000 nm, respectively. From the figure, MOSFETs with larger gate size have significant impact on the overall delay distribution. Thus, ΔV_{T} distribution for the smaller transistor size cannot be extracted accurately from this RO only. One solution can be to use very high size ratios for the skewed inverter. However, the required size ratio is not fixed and may result in a unrealistic value if the RTN is high for the target process. Instead, we propose an iterative statistical method which does not rely on specific size ratios to extract ΔV_{T} distributions. This is performed by modeling the gate size dependency and utilizing the fact that total distribution is a convolution of distributions from smaller and larger transistors.

C. Extraction of ΔV_{T} Distribution

As we obtain delay distributions using RO based test structures, we need to extract ΔV_{T} distributions from measured

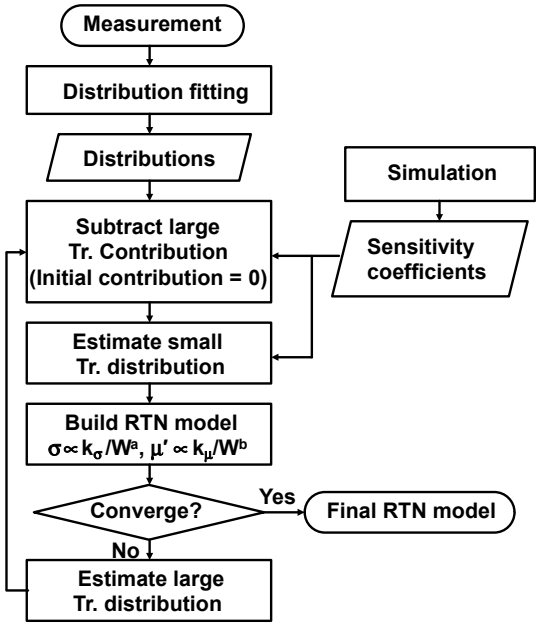


Fig. 3: Proposed characterization flow.

delay distributions. In order to do that, we first approximate total delay variation as follows.

$$\Delta D \approx \sum k_i \Delta V_{\mathrm{T,i}}. \tag{5}$$

Here, k_i is sensitivity coefficient and ΔV_{Ti} is RTN induced ΔV_{T} fluctuation for a particular transistor. Now, if ΔV_{T} follows Lognormal distribution $\ln\mathcal{N}(\mu, \sigma^2)$, then $k_i \Delta V_{\mathrm{T}}$ will follow $\ln\mathcal{N}(\mu + \ln k_i, \sigma^2)$. This refers that for the same transistor size, the delay contribution contributed by transistors of different sensitivity coefficient values can be expressed by Lognormal distributions of the same σ value. As sum of Lognormal distributions can be approximated by another Lognormal distribution, we can derive μ_z and σ_z of the measured delay distribution as in (6) [11, 12].

$$\begin{aligned} \sigma_z^2 &\sim \ln\left((e^{\sigma^2}-1)\frac{\sum k_j^2}{(\sum k_j)^2}+1\right), \\ \mu_z &\sim \mu + \frac{\sigma^2}{2} - \frac{\sigma_z^2}{2} + \ln(\sum k_j). \end{aligned} \tag{6}$$

Thus, measured distribution parameters μ_z and σ_z can be expressed by the terms of μ, σ and k_j. Solving (6) for μ and σ, we obtain these values with (8) . Thus, ΔV_{T} distribution is obtained from ΔD distributions given the sensitivity coefficients of each transistor in the RO.

$$\sigma^2 \sim \ln\left(\frac{\exp(\sigma_z^2)-1}{C_{\mathrm{k1}}}+1\right), C_{\mathrm{k1}} = \frac{\sum k_j^2}{(\sum k_j)^2}, \tag{7}$$

$$\mu \sim \mu_z - \frac{\sigma^2}{2} + \frac{\sigma_z^2}{2} - \ln(\sum k_j). \tag{8}$$

D. RTN Characterization Flow

We propose a modeling methodology shown in Fig. 3 that incorporates RTN contributions from both the smaller and larger transistors. Using Lognormal models to represent the ΔD and ΔV_{T} distributions, convolution and de-convolution of PDFs are used to obtain sum and difference between multiple distributions. An iterative flow is used which update the RTN model at each iteration.

At the beginning of the flow, Lognormal distribution parameters of μ_z and σ_z are fitted with the measured ΔD distribution for each RO. Then, Lognormal distribution parameters of μ and σ of the ΔV_{T} distribution are estimated using (8). In the first iteration, we consider that RTN of each RO is contributed by the smaller transistors only ignoring the larger transistors. Therefore, RTN of each RO is attributed to smaller transistors with different gate sizes. RTN of an RO where pMOSFET is smaller than nMOSFET is attributed to pMOSFET and vice versa. Thus, we obtain Lognormal distribution parameters for different gate sizes of pMOSFET and nMOSFET, respectively. The μ and σ values of ΔV_{T} distributions for each gate size are then fitted against a model that incorporates gate size dependency as shown in (9) and (10).

$$\mu = \ln\hat{\mu} = \ln\left(\frac{k_\mu}{W^{a_\mu}}\right), \tag{9}$$

$$\sigma = \frac{k_\sigma}{W^{a_\sigma}}. \tag{10}$$

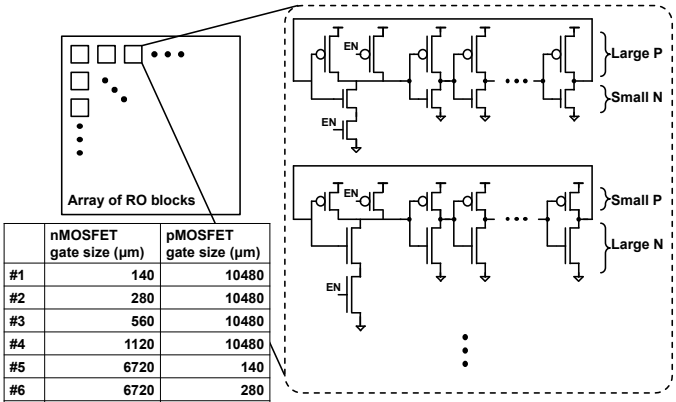
One key point to note in (9) is that logarithm is used to model gate size dependency. This is to make sure that with gate size approaching infinity, ΔV_{T} spread approaches zero. Although contributions from the larger transistors were ignored at the first iteration, these contributions are taken into account since the second iteration forward. We estimate these contributions using the models of (9) and (10) that are obtained at the end of the previous iteration. Since the second iteration forward, as we have estimations for larger transistor contributions, we deduct these contributions and re-evaluate the ΔV_{T} distributions for the smaller transistors. After several iterations, all the distribution parameter values converges to fixed values. Finally, we obtain ΔV_{T} distributions for each transistor size of pMOSFET and nMOSFET. In this study, our flow converges after the fourth iteration.

III. Measurement and Results

A. Test Structure

Fig. 4 shows our test structure in a 65 nm SOTB (Silicon on Thin Body) process consisting of an array of RO blocks. There are 150 blocks in a chip. Therefore, we obtain 150 samples for each RO type. Each block consists of multiple ROs with different skewed inverters. Transistor sizing used in the skewed inverters are shown in the table. There are two types of skewed inverters. One type has smaller nMOSFET and larger pMOSFET. The other type has smaller pMOSFET and larger nMOSFET. Smaller transistor size in each inverter type is varied to four different sizes to evaluate gate size dependency. Fig. 5 shows chip micrograph of our test structure.

As RTN is a time-dependent phenomena, the all RO instances are measured for 12 s of time. The oscillation signal



	nMOSFET gate size (μm)	pMOSFET gate size (μm)
#1	140	10480
#2	280	10480
#3	560	10480
#4	1120	10480
#5	6720	140
#6	6720	280
#7	6720	560
#8	6720	1120
#9	6720	10480

Fig. 4: An array of ROs to evaluate transistor noise of various gate widths.

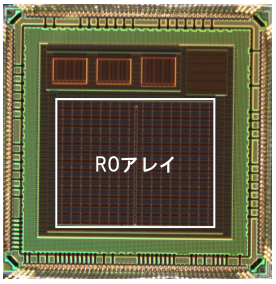


Fig. 5: Chip micrograph.

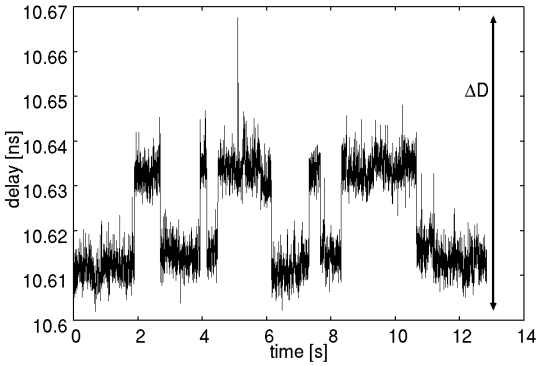


Fig. 6: Sample with large delay fluctuation.

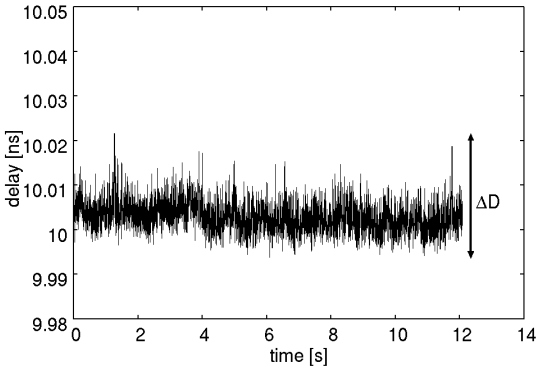


Fig. 7: Sample with small delay fluctuation.

for each circuit is integrated for about 2 ms and then measured with a clock signal of 24 MHz frequency.

B. Delay Distributions

Figs. 6 and 7 shows two samples of oscillation period fluctuation over 12 s of time. Fig. 8 shows measured delay distributions for four ROs where pMOSFET is much smaller than nMOSFET. pMOSFETs of four different sizes are used here. Delay distribution follows Lognormal distribution. Fig. 9 shows delay distributions for ROs with four different nMOSFETs where nMOSFET is much smaller than pMOSFET. In this study, we focus on the total delay variation, thus we do not extract single trap induced RTN. The total delay variation is thus results of both single trap and multiple traps.

C. Characterization Flow

Fig. 10 shows traces of σ values that converge as the number of iteration increases in the cases of four nMOSFET dominated ROs. After three iterations, the values converge to constant values confirming that the proposed iterative flow works.

D. Gate Size Dependency Modeling

As ROs of four different gate sizes nMOSFET and pMOSFET each are used, we obtain four sets of (μ, σ^2) values for nMOSFET and four sets of (μ, σ^2) for pMOSFET. Finally, $\hat{\mu}(= \mathrm{e}^{\mu})$ and σ are plotted and fitted against the gate sizes.

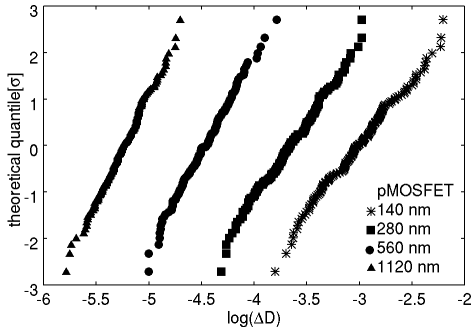


Fig. 8: ΔD distributions for four skewed ROs where pMOSFET is much smaller than nMOSFET.

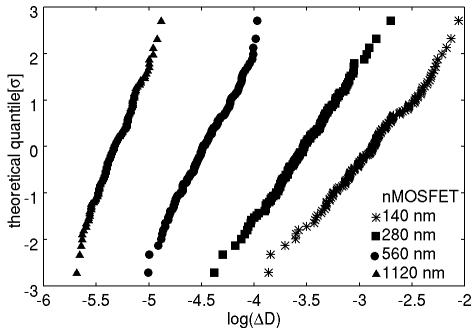


Fig. 9: ΔD distributions for four skewed ROs where nMOSFET is much smaller than pMOSFET.

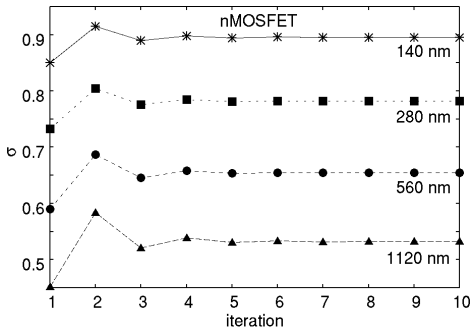


Fig. 10: Change of σ of Lognormal distribution for four different nMOSFETs.

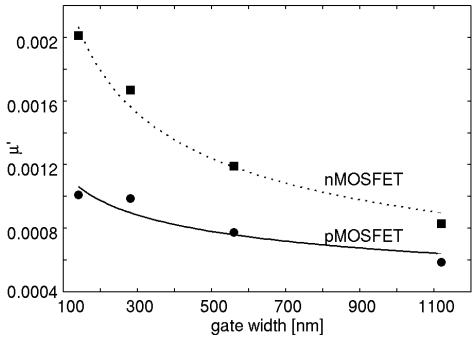


Fig. 11: Gate size dependency of $\hat{\mu}$ for pMOSFET and nMOSFET.

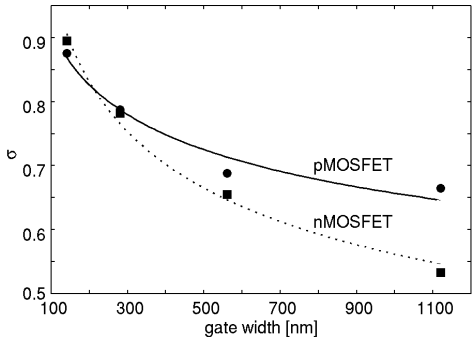


Fig. 12: Gate size dependency of σ for pMOSFET and nMOSFET.

Next, we show the final $\hat{\mu}$ and σ values for pMOSFET and nMOSFET of four different gate sizes. Fig. 11 shows the resulted $\hat{\mu}$ dependency for nMOSFET and Fig. 12 shows the resulted σ for pMOSFET. Solid and dotted lines show the fitted model equations of (9) and (10). We obtain monotonic change of $\hat{\mu}$ and σ values over transistor gate size. The model equations fits the data well. The evaluated $\hat{\mu}$ follows $0.015/W^{0.40}$ and $0.004/W^{0.24}$ for nMOSFET and pMOSFET, respectively. Evaluated σ follows $3.0/W^{0.24}$ and $1.8/W^{0.14}$ for nMOSFET and pMOSFET, respectively.

Figs. 13 and 14 show the estimated ΔV_{T} distributions for four different gate sizes of pMOSFET and nMOSFET respectively. Estimated results show nMOSFET has larger gate size dependency than pMOSFET in this process.

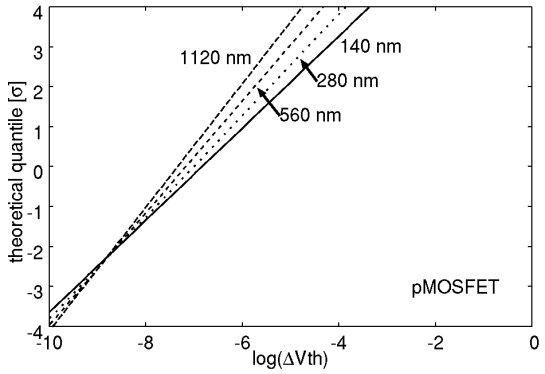


Fig. 13: Estimated ΔV_{T} distributions for four different gate sizes of pMOSFET.

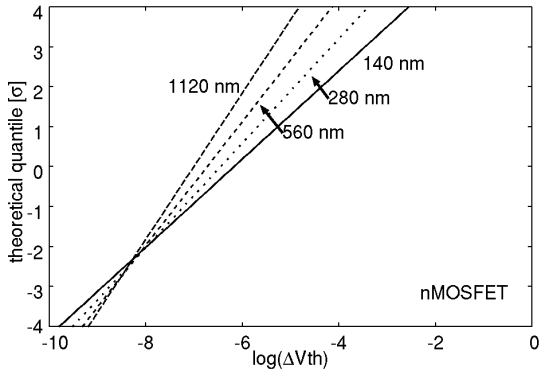


Fig. 14: Estimated ΔV_{T} distributions for four different gate sizes of nMOSFET.

E. Validation

Figs. 15 and 16 show the comparisons between measured and estimated delay distributions for pMOSFET and nMOSFET dominant ROs. Measured and estimated distributions match well. Delay estimations are performed based on the RTN model developed using our proposed methodology.

IV. Conclusion

Ring oscillators (RO) with different skewed inverters can be used to characterize RTN gate size dependency. Although delay distribution of a particular RO type is a convolution of RTN contributions of both the pMOSFET and nMOSFET, we show that an iterative characterization methodology can be effective to estimate pMOSFET and nMOSFET specific RTN models. The characterization flow converges after several iterations that give us RTN models incorporating gate size dependency for pMOSFET and nMOSFET separately. Measurement results from a 65 nm SOTB (Silicon On Thin Body) process confirms that overall delay distribution due to transistor RTN is best represented by Lognormal distributions. Then, RTN models incorporating gate size dependency is used for the two Lognormal distribution parameters. The model is then used to predict the delay distributions for different skewed ROs. Predicted and measured distributions match well. Thus,

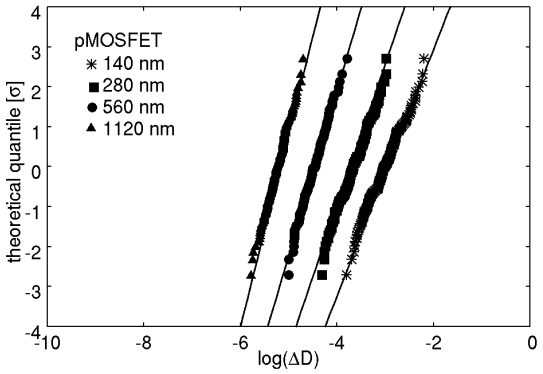


Fig. 15: Comparison between measured and estimated delay distributions for pMOSFET dominated skewed inverters.

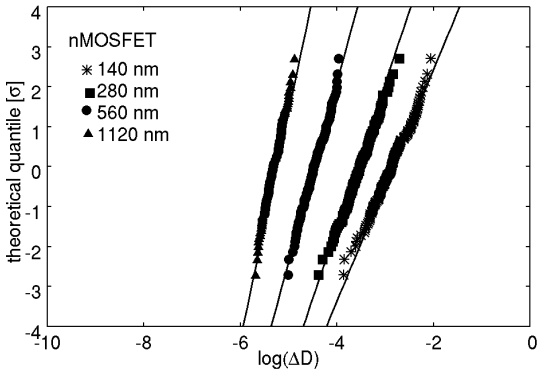


Fig. 16: Comparison between measured and estimated delay distributions for nMOSFET dominated skewed inverters.

the model is useful in analysis of circuit performance that consists of transistors of various gate sizes.

ACKNOWLEDGMENT

The authors would like to express their thanks to Hidenori Gyoten for his support in measurement. The VLSI chip in this study was fabricated in the chip fabrication program of the VLSI Design and Education Center (VDEC), the University of Tokyo, in collaboration with Renesas Electronics. This work has been supported in part by JSPS KAKENHI 25280014 and 16H01713.

REFERENCES

[1] N. Tega, H. Miki, and F. Pagette, "Increasing Threshold Voltage Variation due to Random Telegraph Noise in FETs as Gate Lengths Scale to 20 nm," in *Symposium on VLSI Technology*, 2009, pp. 50–51.

[2] H. Qiu, T. Mizutani, Y. Yamamoto, H. Makiyama, T. Yamashita, H. Oda, S. Kamohara, N. Sugii, T. Saraya, M. Kobayashi, and T. Hiramoto, "Impact of Random Telegraph Noise on Write Stability in Silicon-on-Thin-BOX (SOTB) SRAM Cells at Low Supply Voltage in Sub-0.4V Regime," in *IEEE Symposium on VLSI Technology*, 2015, pp. 38–39.

[3] T. Matsumoto, K. Kobayashi, and H. Onodera, "Impact of Random Telegraph Noise on CMOS Logic Delay Uncertainty under Low Voltage Operation," in *International Electron Devices Meeting*, dec 2012, pp. 25.6.1–25.6.4.

[4] A. Ghetti, C. Compagnoni, A. Spinelli, and A. Visconti, "Comprehensive Analysis of Random Telegraph Noise Instability and Its Scaling in Deca-Nanometer Flash Memories," *IEEE Transactions on Electron Devices*, vol. 56, no. 8, pp. 1746–1752, 2009.

[5] K. Takeuchi, T. Nagumo, S. Yokogawa, K. Imai, and Y. Hayashi, "Single-Charge-Based Modeling of Transistor Characteristics Fluctuations Based on Statistical Measurement of RTN Amplitude," in *Symposium on VLSI Technology*, 2009, pp. 54–55.

[6] J. Zou, R. Wang, S. Guo, M. Luo, Z. Yu, X. Jiang, P. Ren, J. Wang, J. Liu, J. Wu, W. Wong, S. Yu, H. Wu, S. W. Lee, Y. Wang, and R. Huang, "New understanding of state-loss in complex RTN: Statistical experimental study, trap interaction models, and impact on circuits," in *IEEE International Electron Devices Meeting*, 2015, pp. 34.5.1–34.5.4.

[7] S. Fujimoto, A. K. M. M. Islam, T. Matsumoto, and H. Onodera, "Inhomogeneous Ring Oscillator for Within-Die Variability and RTN Characterization," *IEEE Transactions on Semiconductor Manufacturing*, vol. 26, no. 3, pp. 296–305, 2013.

[8] S. Dongaonkar, M. D. Giles, A. Kornfeld, B. Grossnickle, and J. Yoon, "Random Telegraph Noise (RTN) in 14nm Logic Technology : High Volume Data Extraction and Analysis," in *IEEE Symposium on VLSI Technology*, 2016, pp. 176–177.

[9] A. K. M. M. Islam and H. Onodera, "In-Situ Variability Characterization of Individual Transistors Using Topology-Reconfigurable Ring Oscillators," in *International Conference on Microelectronic Test Structures*, 2014, pp. 121–126.

[10] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching Properties of MOS Transistors," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, oct 1989.

[11] L. Fenton, "The Sum of Log-Normal Probability Distributions in Scatter Transmission Systems," *IRE Transactions on Communications Systems*, vol. 8, no. 1, pp. 57–67, March 1960.

[12] N. Beaulieu, A. Abu-Dayya, and P. McLane, "Comparison of Methods of Computing Lognormal Sum Distributions and Outages for Digital Wireless Applications," in *IEEE International Conference on Communications*, May 1994, pp. 1270–1275 vol.3.