# Statistical Analysis and Modeling of Random Telegraph Noise Based on Gate Delay Variation Measurement

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***Abstract*—We propose a characterization and modeling methodology for Random Telegraph Noise (RTN) induced $\Delta V_{\mathrm{th}}$ variation based on gate delay variation measurement. We characterize the total amount of $\Delta V_{\mathrm{th}}$ and model its scaling effect. A topology-reconfigurable ring oscillator (RO) is used to obtain gate delay variations between inverter stages. The devices under test are operated at near- or sub-threshold region to characterize RTN at low supply voltage. Measurement and characterization results from a 65 nm test chip show that lognormal distribution based modeling represents RTN-induced $\Delta V_{\mathrm{th}}$ variability precisely. We extract the model parameters and evaluate the gate size dependency of these parameters. It is found that $\mu_{\mathrm{l}}$ of the lognormal distribution, $\ln\mathcal{N}(\mu_{\mathrm{l}}, \sigma_{\mathrm{l}}^2)$, does not have specific gate size dependency. Whereas, $\sigma$ shows a $W^{-a}$ dependency to gate size rather than the commonly assumed $W^{-1}$ dependency, where $a$ is evaluated to be less than 0.5. The proposed comprehensive statistical model and its parameter dependency is suitable for performance analysis of circuits where transistors of different gate sizes are used.**

## I. Introduction

As the scaling of transistor dimensions continues, variability between the transistors poses more challenge on designing reliable computing systems. With the emergence of IoT (Internet of Things), the need for energy-efficient computing is more demanding now. Supply voltage lowering is the most effective way to increase energy efficiency, but the effect of variability also becomes severe as the circuit performance is now more sensitive to variation. With transistor scaling, variability such as process variation and random telegraph noise (RTN) are reported to increase [1, 2]. In order to deal with variability, the variability needs to be accurately expressed by suitable statistical distributions, and the parameters of the distribution need to model the scaling effects such as gate size.

A common technique to deal with process variation is to up-size the devices. However, up-sizing also increase energy consumption, thus inaccurate statistical models or over pessimism can increase energy consumption by several magnitudes. The Pelgrom model [3], which relates the amount of random process variability to channel area, helps designers to optimize their designs to avoid unnecessary over-sizing. RTN induced $V_{\mathrm{th}}$ variation is also a statistical phenomena and have a strong gate size dependency. Unlike process variation, RTN-induced $\Delta V_{\mathrm{th}}$ distribution is reported to have long tails in the distributions. Therefore, a suitable statistical model and its parameter extraction are required to account for RTN-induced $\Delta V_{\mathrm{th}}$ variability during the design phase.

There are previous reports of characterization and modeling of RTN induced $V_{\mathrm{th}}$ variation [4–6]. The most common and basic approach is transistor $I$–$V$ measurement approach. This approach uses $g_{\mathrm{m}}$ to convert $\Delta I_{\mathrm{D}}$ to $\Delta V_{\mathrm{th}}$. However, $I$–$V$ based approach has the following limitations. Firstly, constant bias is applied which is not representative of the actual switching condition in a logic circuit. Although static $I$–$V$ based model was very useful for the random process variation, the dynamic nature of RTN, however, requires the verification from in-situ characterization under switching conditions. Secondly, the literature reports often use gate bias much higher where the transistor is in strong inversion. However, at low supply voltage, the transistors operate at weak or moderate inversion. At near-threshold operation, RTN induced $\Delta V_{\mathrm{th}}$ is reported to increase [7], thus requires the modeling based on transistors operating near $V_{\mathrm{th}}$. Finally, statistics of the number of traps and $\Delta V_{\mathrm{th}}$ due to each trap are the target of characterization. Overall $\Delta V_{\mathrm{th}}$ that a transistor can counter during the operation are calculated from a complex probabilistic computation. From circuit designers' perspectives, however, comprehensive modeling of overall $\Delta V_{\mathrm{th}}$ due to RTN is required instead of single trap based $\Delta V_{\mathrm{th}}$ modeling. Furthermore, confirmation from measurement that whether total $\Delta V_{\mathrm{th}}$ estimation from single trap $\Delta V_{\mathrm{th}}$ is valid or not. To overcome the above limitations, this paper proposes an in-situ characterization and modeling methodology of RTN for devices operating under switching condition. Weak or moderate inversion region is targeted to model RTN for low supply voltage operation.

In Sec. II, we describe our proposed statistical modeling approach of $\Delta V_{\mathrm{th}}$ variation due to RTN. In Sec. III, we describe a RTN characterization methodology from delay variation measurement. Sec. IV demonstrates measurement and characterization results. In Sec. V, we put our concluding remarks.

## II. Statistical Modeling of RTN

Static process variation of $V_{\mathrm{th}}$ is reported to follow normal distribution, $\mathcal{N}(\mu_{\mathrm{n}}, \sigma_{\mathrm{n}}^2)$ [1]. The scaling effect of static random variation can be well expressed by the following Pelgrom model [3].

$$\sigma_{V_{\mathrm{th}}} = \frac{A_{V_{\mathrm{th}}}}{\sqrt{WL}}, \quad (1)$$

where, $W$ is gate width and $L$ is gate length. $A_{V_{\mathrm{th}}}$ consists of process parameters, and normally is considered constant for same channel profiles. So, once $A_{V_{\mathrm{th}}}$ is characterized for a process, the circuit designers simply need to use Eq. (1) to analyze the circuit performance variations. However, RTN induced $V_{\mathrm{th}}$ variations are reported to have long tails in the distribution and therefore normal distribution can not be used to model these variations [4–7]. Literature reports suggest two distributions to model RTN induced $V_{\mathrm{th}}$ variation. One is the exponential distribution, $\mathrm{Exp}(\sigma_{\mathrm{e}})$, and the other is the

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TABLE I: Key characteristics of and symbols used for different distributions.

| | Normal | Lognormal | Exponential |
|---|---|---|---|
| Parameters | $\mu_{\mathrm{n}}, \sigma_{\mathrm{n}}^2$ | $\mu_{\mathrm{l}}, \sigma_{\mathrm{l}}^2$ | $\sigma_{\mathrm{e}}$ |
| PDF | $\frac{1}{\sigma_{\mathrm{n}}\sqrt{2\pi}} \mathrm{e}^{-\frac{(x-\mu_{\mathrm{n}})^2}{2\sigma_{\mathrm{l}}^2}}$ | $\frac{1}{x\sigma_{\mathrm{l}}\sqrt{2\pi}} \mathrm{e}^{-\frac{(\ln x-\mu_{\mathrm{l}})^2}{2\sigma_{\mathrm{l}}^2}}$ | $\frac{1}{\sigma_{\mathrm{e}}} \mathrm{e}^{-\frac{x}{\sigma_{\mathrm{e}}}}$ |
| CDF | $\frac{1}{2}\left[1+\mathrm{erf}\left(\frac{x-\mu_{\mathrm{n}}}{\sigma_{\mathrm{n}}\sqrt{2}}\right)\right]$ | $\frac{1}{2}\left[1+\mathrm{erf}\left(\frac{\ln x-\mu_{\mathrm{l}}}{\sigma_{\mathrm{l}}\sqrt{2}}\right)\right]$ | $1-\mathrm{e}^{-\frac{x}{\sigma_{\mathrm{e}}}}$ |
| Mean | $\mu_{\mathrm{n}}$ | $\mathrm{e}^{\mu_{\mathrm{l}}+\sigma_{\mathrm{l}}^2/2}$ | $\sigma_{\mathrm{e}}$ |
| Variance | $\sigma_{\mathrm{n}}^2$ | $(\mathrm{e}^{\sigma_{\mathrm{l}}^2}-1)\mathrm{e}^{2\mu_{\mathrm{l}}+\sigma_{\mathrm{l}}^2}$ | $\sigma_{\mathrm{e}}^2$ |
| Sum of distribution | Normal | Approx. lognormal at right tail | Gamma |

lognormal distribution, $\ln\mathcal{N}(\mu_{\mathrm{l}}, \sigma_{\mathrm{l}}^2)$. 3-D CAD simulations and device measurements are performed to investigate the scaling effect into the above statistical model parameters [4–6]. Key characteristics of the three distributions of normal, exponential and lognormal are shown in Table I.

There are many reports in the literature on statistical modeling of RTN and its scaling effects. Distribution of single-trap induced $\Delta V_{\mathrm{th}}$ is reported to follow exponential distribution [4, 5, 7]. Scaling effect of the model parameter of the exponential distribution is reported to follow $W^{-1}L^{-0.5}$. Multi-trap induced overall $\Delta V_{\mathrm{th}}$ fluctuation is believed to be a superimpose of the amounts of each single-trap induced $\Delta V_{\mathrm{th}}$ . Overall $\Delta V_{\mathrm{th}}$ is obtained by combining the statistics of the number of traps with the statistics of single-trap amplitudes, $\Delta V_{\mathrm{th}}$, into one comprehensive statistical model [6]. $95\%$ percentile of overall $\Delta V_{\mathrm{t}}$ distribution is reported to have $W^{-1}L^{-1.5}$ dependency [6]. However, it is still not clear which distribution best expresses the overall $\Delta V_{\mathrm{th}}$ variation, and how the model parameters relate to transistor parameters of gate width for example. Next, at near-threshold operation and under switching condition, the overall $\Delta V_{\mathrm{th}}$ distribution is not yet characterized and modeled. In this paper, we perform characterization and analysis of RTN-induced $\Delta V_{\mathrm{th}}$ variation based on delay variation measurements, and extract model parameters and its scaling effects. We perform a comparative analysis of RTN induced $\Delta V_{\mathrm{th}}$ variation using both of the exponential and lognormal distribution and show that lognormal distribution represents RTN more precisely. Next, we characterize and model gate size dependency into the model parameters. We find that the scaling effect is much smaller than those reported in the literature which will be discussed in Sec. IV.

## III. RTN Characterization Methodology

### A. Characterization Methodology

In order to perform in-situ delay variation to model RTN for logic circuits, an RO based approach is useful. However, characterization of RTN-induced $\Delta V_{\mathrm{th}}$ distribution from conventional RO based delay measurement is difficult because delay variations of multiple inverter stages are averaged out. Conventional RO based characterization is useful when the underline distribution is known. However, when investigating the best distribution that represent $\Delta V_{\mathrm{th}}$ distribution due to RTN, the above approach faces several limitations and direct visibility into the gate-level distribution is required. In order to overcome this problem, we use a topology-reconfigurable RO

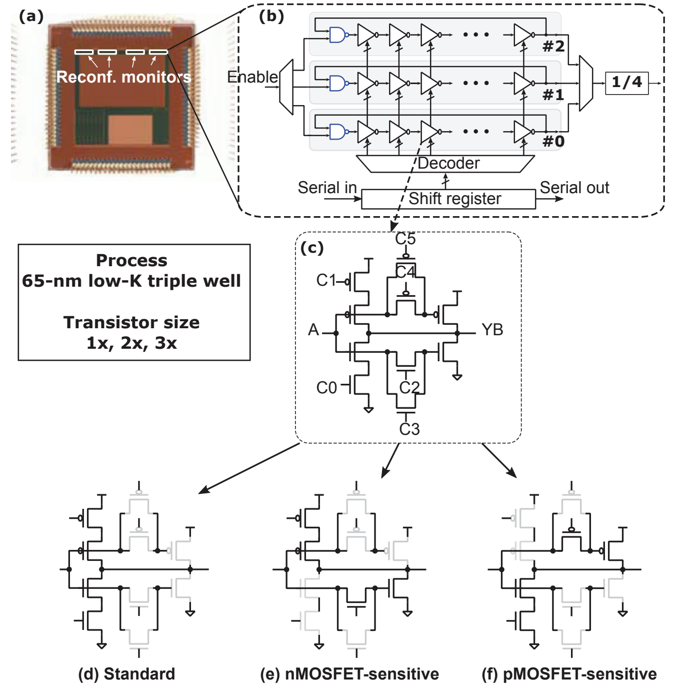



Fig. 1: Topology-reconfigurable ROs for gate delay variation measurement implemented in a 65-nm test chip. ROs with three different gate sizes of 120 nm, 240 nm and 360 nm are implemented for gate size dependency extraction.

TABLE II: Gate sizes used for gate size dependency extraction.

| RO Index | nMOS gate width [nm] | pMOS gate width [nm] |
|---|---|---|
| #0 | 120 | 120 |
| #1 | 240 | 360 |
| #2 | 360 | 240 |

[8]. The topology-reconfigurable RO enables gate-level delay evaluation. In the topology-reconfigurable RO, each inverter delay is configured to have multiple times higher sensitivity than the other stages. The higher sensitivity is utilized to extract variation for each inverter stage. Furthermore, making the inverter delay sensitive to only nMOSFET or pMOSFET provides independent nMOSFET and pMOSFET characterization.

Fig. 1 shows our test chip which comprises four modules with each consisting of three topology reconfigurable ROs. Three different gate sizes are implemented for gate size dependency characterization. The gate sizes are shown in Table II. Each RO is 127 staged. First stage is an NAND gate to turn ON and OFF the oscillation, and the last stage is used as buffer. From a single RO, 125 samples for nMOSFET and 125 measurement samples for pMOSFET are measured by reconfiguring the topology of each stage. Six control signals are used to reconfigure the topology to achieve the following delay characteristics.

1) Equal rise/fall delay as shown in Fig. 1(a),
2) larger fall delay sensitive to nMOS as shown in

Fig. 1(b), and

3) larger rise delay sensitive to pMOS as shown in Fig. 1(c).

### B. Delay Variation Characterization

The delay variation between inverter stages are obtained by the following way. The RO period when the $j$th inverter have higher fall or rise delay sensitivity is expressed as follows.

$$= D_0^j + d^j. \tag{2}$$

Here, $d^j$ is the inverter fall or rise delay for the $j$th stage, and $N$ is the number of stages. $D_0^j$ is the delay contribution from all the inverter delays except the $j$th stage fall delay. Thus, the delay of the target $j$th stage is obtained as follows.

$$d^j = D^j - D_0^j. \tag{3}$$

Although we can only measure $D^j$ with our circuit, for a sufficiently large number of stages, $D_0^j$ can be approximated with $D_0$ which is the delay when all the inverter stages are configured as in Fig. 1(d). If $D_0$ does not show any fluctuation due to RTN, that is does not show any binary fluctuation, then the delay fluctuation observed in $\Delta D^j$ can be attributed to $d^j$ fluctuation. As a result, $\Delta d^j$ is evaluated by measuring $\Delta D^j$.

$$\Delta d^j \approx \Delta D^j. \tag{4}$$

In summary, $(D^j - D_0)$ gives the static process variation for the $j$th stage, and $\Delta D^j$ over time gives the RTN induced fluctuation for the same $j$th stage.

### C. Delay Model

The gate delay of nMOSFET- or pMOSFET-sensitive inverter topology is contributed by two transistors. Thus, the delay fluctuation $\Delta D$ can be expressed by the sensitivity coefficients as follows.

$$\Delta D = k_1 \Delta V_{\mathrm{th1}} + k_2 \Delta V_{\mathrm{th2}}. \tag{5}$$

In our circuit topology, $\alpha = k_2/k_1$ is a constant which depends on the technology parameters of body-effect and DIBL coefficients [9]. Thus, $\Delta V_{\mathrm{th}}$ variation can be evaluated by the following equation.

$$\frac{\Delta D}{k_1} = \Delta V_{\mathrm{th1}} + \alpha \Delta V_{\mathrm{th2}}. \tag{6}$$

### D. $\Delta V_{\mathrm{th}}$ Characterization

Delay variation, $\Delta D$, is converted to $\Delta V_{\mathrm{th}}$ using sensitivity coefficient, $k_1$.

$$k_1 = \left(\frac{\partial d^j}{\partial V_{\mathrm{th}}}\right)_{d^j = d^j_{\mathrm{meas}}} = \left(\frac{\partial \Delta D^j}{\partial V_{\mathrm{th}}}\right)_{\Delta D^j = \Delta D^j_{\mathrm{meas}}}. \tag{7}$$

Here, $d^j_{\mathrm{meas}}$ is inverter delay obtained using Eq. (3). The sensitivity value is calculated by transistor-level simulation using the foundry provided transistor model. At near- and sub-threshold operation, as inverter delay is non-linear to $V_{\mathrm{th}}$ variation, the sensitivity is not constant. Thus, sensitivity value at the actual $V_{\mathrm{th}}$ value in silicon need to be estimated. Thanks to our reconfigurable circuit topology, the $V_{\mathrm{th}}$ value for each inverter stage can be referred from the delay value which is shown in Fig. 2. From the delay model of Eq. (5), $\Delta d/k_1$ does not give the $\Delta V_{\mathrm{th}}$ in a single MOSFET, rather the total $\Delta V_{\mathrm{th}}$ contribution from the two MOSFETs. Single MOSFET $\Delta V_{\mathrm{th}}$ can be decomposed assuming a statistical distribution model such as the lognormal distribution. Using Fenton's method [10], $\mu_{1,\Delta V_{\mathrm{th}}}$ and $\sigma^2_{1,\Delta V_{\mathrm{th}}}$ are computed from Eq. (6) with the following equations.

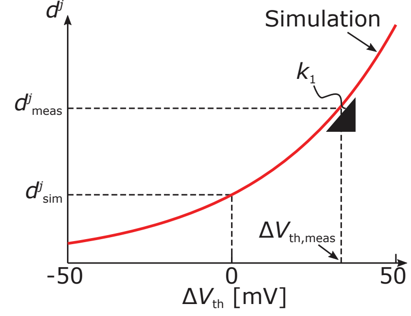



Fig. 2: Sensitivity coefficient calculation by model-hardware correlation.

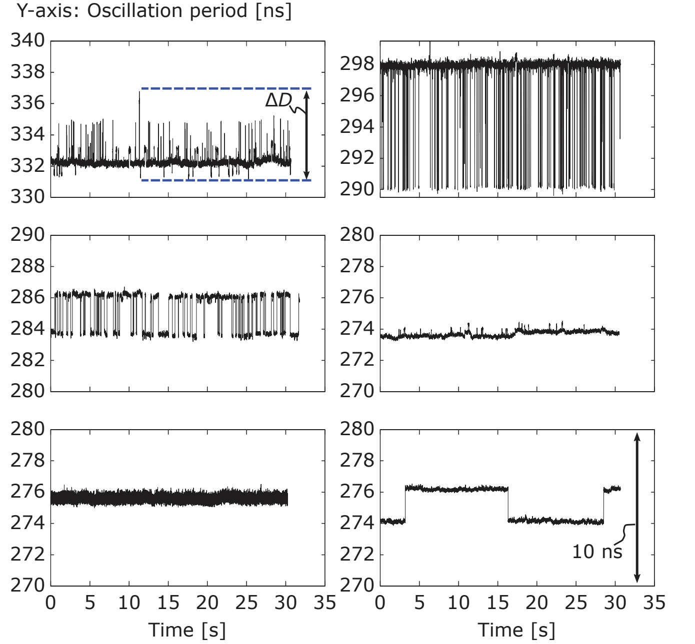



Fig. 3: Several samples of observed RTN-induced delay fluctuations for different pMOS-sensitive inverters.

$$\sigma^2_{1,\Delta V_{\mathrm{th}}} = \ln\left[\frac{(1+\alpha)^2 \exp(\sigma^2_{\frac{\Delta D}{k_1}}) - 2\alpha}{1+\alpha^2}\right], \tag{8}$$

$$\mu_{1,\Delta V_{\mathrm{th}}} = \mu_{\frac{\Delta D}{k_1}} - \frac{\sigma^2_{\Delta V_{\mathrm{th}}}}{2} - \ln(1+\alpha) + \frac{\sigma^2_{\frac{\Delta D}{k_1}}}{2}. \tag{9}$$

## IV. Measurement and Analyses

### A. Measurement

In order to evaluate inverter delay operating at near- or sub-threshold region, supply voltage of 0.8 V is used. Because of

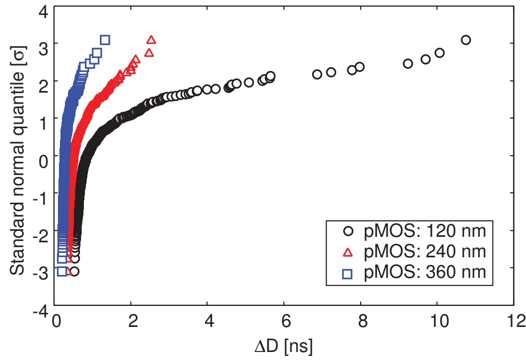



Fig. 4: Q-Q plot of pMOSFET-sensitive gate delay.

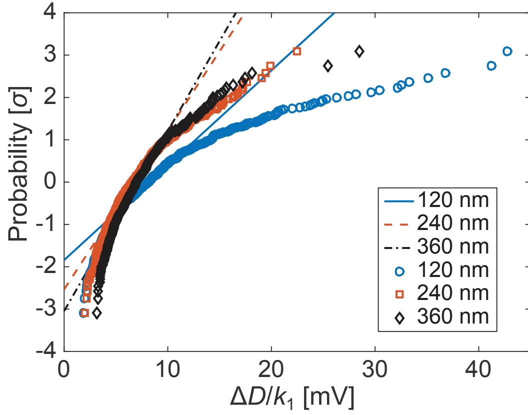



Fig. 5: Probability plot for normal distribution of pMOSFET $\Delta D/k_1$.

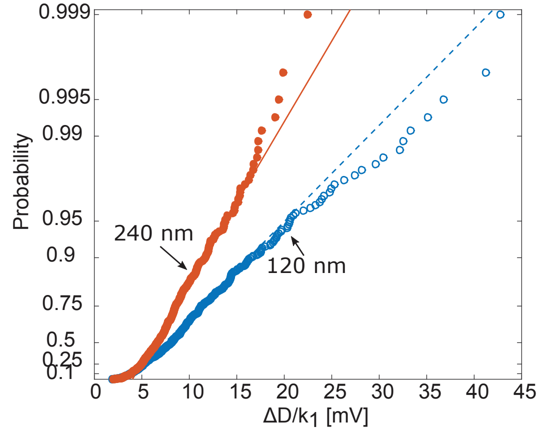



Fig. 6: Probability plot for exponential distribution of pMOSFET $\Delta D/k_1$.

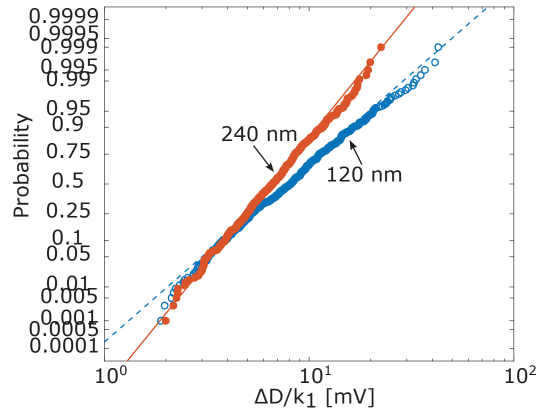



Fig. 7: Probability plot for lognormal distribution of pMOSFET $\Delta D/k_1$.

the $V_{\mathrm{th}}$ drop across the pass-gate transistor, the gate overdrive for the pull-up or pull-down transistor in inhomogeneous stage is around transistor $V_{\mathrm{th}}$. In other words, for each inhomogeneous configuration, only the devices under test operate near $V_{\mathrm{th}}$ and all the other devices operate above $V_{\mathrm{th}}$. Four ROs are measured for both of the nMOSFET and pMOSFET $V_{\mathrm{th}}$ characterizations. As a result, a total of $125 \times 4 = 500$ measurement samples are obtained for each gate width. For each RO, oscillation frequency is measured over 35 s with an integration time of 1 ms.

Fig. 3 shows measurement samples of oscillation period observed over time for six different inhomogeneous configurations. The measurement results correspond to pMOSFET RTN-induced $\Delta V_{\mathrm{th}}$. Discrete fluctuations in the oscillation periods are observed which confirms the characteristics of RTN. We can observe RTN of various amplitudes, time constants and multiple traps. Here we focus on the total amount of delay fluctuation that can occur during the circuit operation. Thus, the following definition of delay fluctuation is used to evaluate overall $\Delta V_{\mathrm{th}}$.

$$\Delta D = D_{\mathrm{max}} - D_{\mathrm{min}} = 1/F_{\mathrm{min}} - 1/F_{\mathrm{max}}. \qquad (10)$$

### *B. Distribution Fitting*

Fig. 4 shows a probability plot for normal distribution of the observed gate-delay fluctuation for three different channel sizes using pMOSFET-sensitive inhomogeneous topology. As expected, long tails are observed in all the three distributions. Next, the delay distribution is converted to $\Delta D/k_1$ distribution. $\Delta D/k_1$ distributions for three different gate widths are shown in Fig. 5. The figure confirms that long tails exist at $\Delta V_{\mathrm{th}}$ level distributions, as $\Delta D/k_1$ represents sum of two $\Delta V_{\mathrm{th}}$ distributions as shown in Eq. (6).

Next, we plot the measured $\Delta D/k_1$ distributions for exponential and lognormal distributions to examine which distribution represents RTN induced $\Delta V_{\mathrm{th}}$ variation best. Fig. 6 shows the probability plot for exponential distribution, whereas Fig. 7 shows the probability plot for lognormal distribution. From the figures, we observe that both the exponential and the lognormal distributions represent the measured data quite well. In order to further examine which of the distributions is better to represent the data, cumulative probability function plot is shown in Fig. 8. Lognormal distribution fits the empirical CDF of measured data better. Thus, we conclude that lognormal distribution suits better at modeling the overall $\Delta V_{\mathrm{th}}$ variation due to RTN.

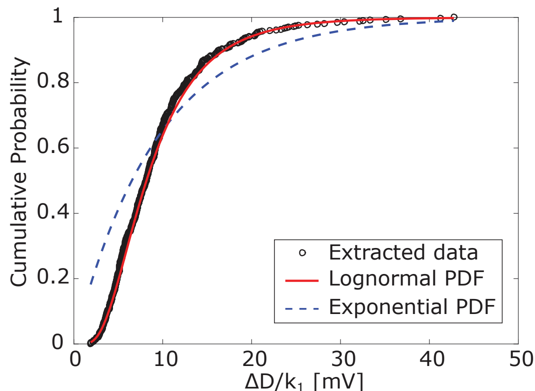
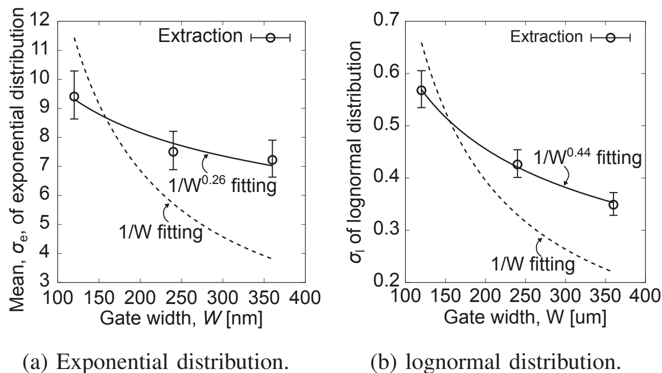



Fig. 8: Comparison between empirical, exponential and lognormal CDFs of $\Delta D/k_1$ for pMOSFET of 120 nm gate width.



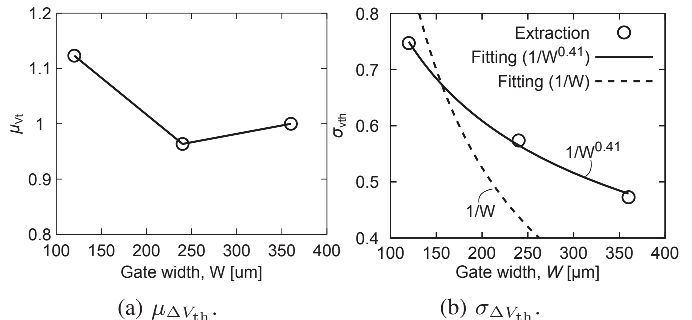

(a) Exponential distribution. (b) lognormal distribution.

Fig. 9: Gate size dependency of $\sigma_{\rm e}$ and $\sigma_{\rm l}$ parameters of $\Delta D/k_1$ for exponential and lognormal distributions.

### C. Modeling of Gate Size Dependency

Next, gate size dependency of $\Delta D/k_1$ are evaluated. Fig. 9(a) shows the extracted $\sigma_{\rm e}$ with an error bar showing the bounds of a 95% confidence interval for exponential distribution. The exponential distributions are obtained by fitting $\sigma_{\rm e}$ to the measured $\Delta D/k_1$ data. The figure also shows two fitted curves. One uses a $W^{-1}$ model and the other uses a $W^{-a}$ model. $W^{-a}$ model fits the gate size dependency well, and surprisingly the value of $a$ is only 0.26 which is much smaller than the commonly assumed value of 1. Fig. 9(b) shows the fitted $\sigma_{\rm l}$ of lognormal distributions against the gate sizes. $W^{-a}$ model fits the gate size dependency best and the value of $a$ is 0.44.

Assuming $\Delta V_{\rm th}$ distribution due to RTN follows lognormal distribution, we calculated the $\mu_{{\rm l},V_{\rm th}}$ and $\sigma_{{\rm l},V_{\rm th}}$ using Eq. (8) and (9). Extracted $\mu_{{\rm l},V_{\rm th}}$ and $\sigma_{{\rm l},V_{\rm th}}$ values are shown in Figs. 10(a) and 10(b). $\mu_{{\rm l},V_{\rm th}}$ shows no clear dependency on transistor channel size but remain almost same. However, $\sigma_{{\rm l},V_{\rm th}}$ shows monotonous decrease with the increase of channel area. Gate size dependency of $\sigma_{{\rm l},V_{\rm th}}$ is then extracted by fitting to $W^{-a}$ model. It is found that $\sigma_{{\rm l},V_{\rm th}}$ is proportional to $1/W^{0.41}$ rather than $1/W$. From the results, it is confirmed first that lognormal distribution is suitable for modeling RTN. Second, the gate size dependency of the overall $\Delta V_{\rm th}$ have different




(a) $\mu_{\Delta V_{\rm th}}$. (b) $\sigma_{\Delta V_{\rm th}}$.

Fig. 10: Gate size dependency of $\mu_{\rm l}$ and $\sigma_{\rm l}$ parameters of $\Delta V_{\rm th}$ distribution for lognormal distribution.

TABLE III: Extracted model parameters for RTN-induced $\Delta V_{\rm th}$ distribution of different transistor sizes.

| | pMOS | | | nMOS |
|---|---|---|---|---|
| | 120 nm | 240 nm | 360 nm | 360 nm |
| $\mu_{\frac{\Delta D}{k_1}}$ | 2.1 | 1.9 | 2.0 | 1.4 |
| $\sigma_{\frac{\Delta D}{k_1}}$ | 0.57 | 0.43 | 0.35 | 0.38 |
| $\mu_{\Delta V_{\rm th}}$ | 1.1 | 0.96 | 1.0 | 0.51 |
| $\sigma_{\Delta V_{\rm th}}$ | 0.75 | 0.57 | 0.47 | 0.51 |

scaling effects than those reported in the literature. Table III summarizes the extracted parameters for fitted lognormal distributions of $\Delta V_{\rm th}$ variations for different gate width.

Next, $\Delta V_{\rm th}$ distributions for nMOSFET and pMOSFET with the same gate size are compared. Fig. 11 shows the probability plot for exponential distribution of $\Delta D/k_1$ for nMOS and pMOS transistors with gate width of 360 nm. Fig. 12 shows the probability plot for lognormal distribution of $\Delta D/k_1$ for nMOS and pMOS transistors with gate width of 360 nm. As with the case for different gate sizes, $\Delta V_{\rm th}$ distributions for nMOSFET and pMOSFET are well represented by both the exponential and lognormal distributions. When exponential distribution is used, $\sigma_{\rm e}$ values differ largely. However, $\sigma_{\rm l}$ of lognormal distribution shows similar values between them and $\mu_{\rm l}$ differs.

Finally, Fig. 13 shows the projection of $\Delta V_{\rm th}$ distribution based on the extracted model parameters for evaluation of worst-case $\Delta V_{\rm th}$ against device sizing. Gate size of 120 nm shows 60 mV and 128 mV of $\Delta V_{\rm th}$ at $4\sigma$ and $5\sigma$ levels. So, if the RTN follows lognormal distribution up to $4\sigma$ level, special care needs to be taken for designing reliable systems operating at near- or sub-threshold region.

## V. Conclusion

We have presented a characterization methodology of size dependency on overall threshold voltage fluctuation due to RTN for statistical modeling. Our methodology utilizes a topology-reconfigurable ring oscillator for in-situ RTN measurement under switching condition. From the measurement results with a 65-nm test chip, it is observed that lognormal distribution represents $\Delta V_{\rm th}$ variation due to RTN better than the exponential distribution. Size dependency of $\mu_{\rm l}$ and $\sigma_{\rm l}$ of

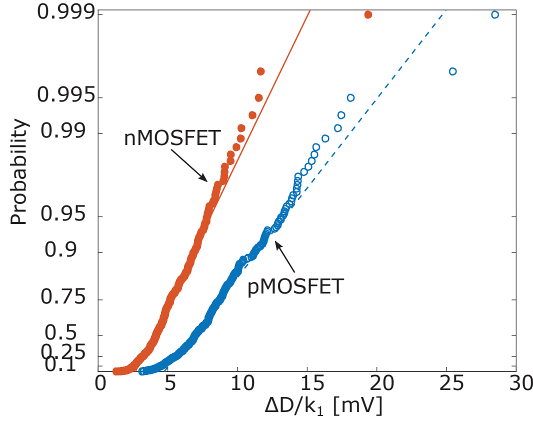


Fig. 11: Probability plot for exponential distribution of the measured $\Delta D/k_1$ against nMOSFET and pMOSFET. Transistor gate width is 360 nm.

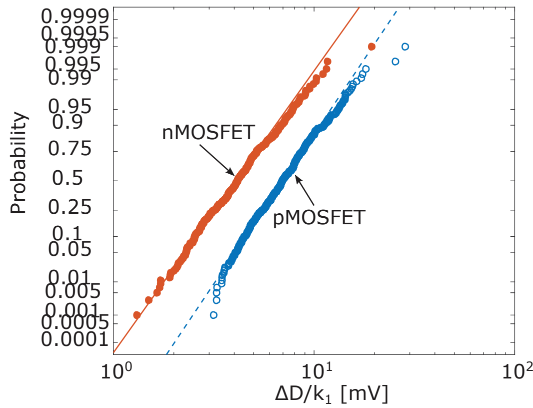


Fig. 12: Probability plot for lognormal distribution of the measured $\Delta D/k_1$ against nMOSFET and pMOSFET. Transistor gate width is 360 nm.

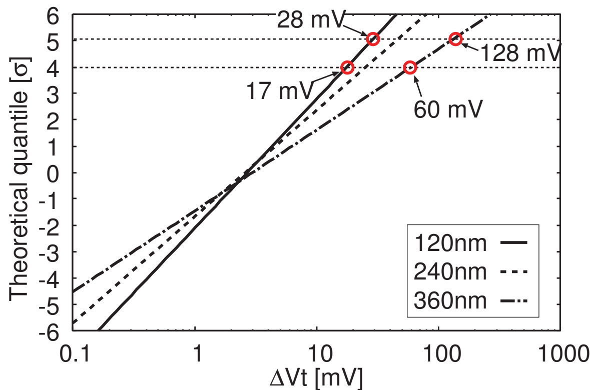


Fig. 13: Prediction of worst-case $\Delta V_{\mathrm{th}}$ due to RTN for three different pMOS transistors.

lognormal distribution for pMOS transistor are extracted. It is found that $\mu_l$ does not have any size dependency but $\sigma_l$ has a $W^{-a}$ relationship to the gate size rather than the commonly assumed $W^{-1}$ relationship. The value of $a$ was evaluated to be less than 0.5. The characterization of gate size dependency on overall $\Delta V_{\mathrm{th}}$ distribution is helpful in establishing compact statistical model for analysis of circuits where various gate sizes are used.

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## References


[1] T. Tsunomura, A. Nishida, F. Yano, A. T. Putra, K. Takeuchi, S. Inaba, S. Kamohara, K. Terada, T. Hiramoto, and T. Mogami, "Analyses of 5$\sigma$ Vth Fluctuation in 65nm-MOSFETs using Takeuchi Plot," in *Symposium on VLSI Technology*, 2008, pp. 156–157.

[2] N. Tega, H. Miki, and F. Pagette, "Increasing Threshold Voltage Variation due to Random Telegraph Noise in FETs as Gate Lengths Scale to 20 nm," in *Symposium on VLSI Technology*, 2009, pp. 50–51.

[3] M. Pelgrom, A. Duinmaijer, and A. Welbers, "Matching Properties of MOS Transistors," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, oct 1989.

[4] K. Takeuchi, T. Nagumo, S. Yokogawa, K. Imai, and Y. Hayashi, "Single-Charge-Based Modeling of Transistor Characteristics Fluctuations Based on Statistical Measurement of RTN Amplitude," in *Symposium on VLSI Technology*, 2009, pp. 54–55.

[5] A. Ghetti, C. Compagnoni, A. Spinelli, and A. Visconti, "Comprehensive Analysis of Random Telegraph Noise Instability and Its Scaling in Deca-Nanometer Flash Memories," *IEEE Transactions on Electron Devices*, vol. 56, no. 8, pp. 1746–1752, 2009.

[6] S. Realov and K. L. Shepard, "Analysis of Random Telegraph Noise in 45-nm CMOS Using On-Chip Characterization System," *IEEE Transactions on Electron Devices*, vol. 60, no. 5, pp. 1716–1722, may 2013.

[7] J. Franco, B. Kaczer, M. Toledano-Luque, P. J. Roussel, J. Mitard, L. Å. Ragnarsson, L. Witters, T. Chiarella, M. Togo, N. Horiguchi, G. Groeseneken, M. F. Bukhori, T. Grasser, and A. Asenov, "Impact of single charged gate oxide defects on the performance and scaling of nanoscaled FETs," in *IEEE International Reliability Physics Symposium*, 2012, pp. 1–6.

[8] A. M. Islam and H. Onodera, "In-Situ Variability Characterization of Individual Transistors Using Topology-Reconfigurable Ring Oscillators," in *International Conference on Microelectronic Test Structures*, 2014, pp. 121–126.

[9] ——, "Sensitivity-independent Extraction of Vth Variation Utilizing Log-normal Delay Distribution," in *International Conference on Microelectronic Test Structures*, 2015, pp. 212–217.

[10] L. F. Fenton, "The Sum of Log-Normal Probability Distributions in Scatter Transmission Systems," *IRE Transactions on Communications Systems*, vol. 8, no. 1, pp. 57–67, 1960.