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In-Situ Variability Characterization of Individual Transistors Using Topology-Reconfigurable Ring Oscillators

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***Abstract*—We propose a variability characterization methodology using a topology-reconfigurable ring oscillator (RO) which enables in-situ characterization of individual transistors in the RO. By configuring the topology-reconfigurable RO into several nMOSFET and pMOSFET-sensitive topologies, local variation of each of the MOSFETs can be estimated. Measurement and estimation results from a 65 nm test chip confirm the validity of our proposed technique. We have successfully characterized static variation as well as RTN induced threshold voltage fluctuation of individual transistors. The proposed methodology can be used for fast and accurate characterization of variability.**

I. Introduction

Accurate characterization of static transistor variability as well as dynamic transistor variability such as RTN (Random Telegraph Noise) and NBTI (Negative Bias Temperature Instability) is the key to reliable and energy-efficient circuit design. Transistor array based I–V measurement where DC bias is applied is performed to characterize these variations [1]. However, this method requires huge time and effort, thus relate to high cost. Several methods are proposed for fast characterization of process variation [2]. However, measuring other variations such as RTN requires different measurement methods. Ring oscillators (RO) can be used for fast characterization of MOSFET variations [3–7]. RO based method has low implementation and measurement cost. In the case of RO, the oscillation frequency is measured and analyzed to extract various variation information. Conventional RO structure where an inverter or nand gate is used as inverting gates gives us a general view on the process characteristics and variations. This limited information is not suitable for detailed characterization of both of the nMOSFET and pMOSFET. Various inverter structures are proposed to change the RO frequency sensitivity to a particular variation source to characterize variations accurately [3–5].

In the scaled process, transistor level variation is becoming dominant. RTN induced variation is expected to be larger than the within-die (WID) variation since 32 nm process [8]. NBTI induced device performance degradation has long been considered as a major reliability concern [9]. These variations need to be characterized and modeled accurately in order to estimate circuit performance accurately. Transistor level variability measurement and characterization will allow us to characterize variations accurately. Conventional RO based characterization fails to give us transistor level characterization. The concept of inhomogeneous structure of RO is proposed to make the RO frequency highly sensitive to only a particular set of transistors. This structure provides us enhanced visibility on transistor level behavior, thus advances the characterization technology. However, measurement of individual transistors is still not possible with this structure.

In order to overcome the above problems, a topology-reconfigurable RO structure is proposed where transistor-by-transistor variability becomes visible [10, 11]. This paper develops an estimation and characterization methodology by which variability of each transistor in the RO can be characterized. This will give us direct insight into transistor-by-transistor characteristics, thus accurate characterization can be possible. Extracting variability of each nMOSFET and pMOSFET has the following advantages. Firstly, the proposed method provides accurate characterization of both of the static and dynamic variations of each transistor. Secondly, it allows to characterize statistical properties as well as relationship between several variability sources.

The remainder of the paper is organized as follows. Topology-reconfigurable RO structure and its operation is explained in Sec. II. We develop our proposed in-situ characterization methodology in Sec. III. Measurement and characterization results from a 65 nm test chip are discussed in Sec. IV. Finally, we conclude the paper in Sec. V.

II. Topology-reconfigurable RO

A topology-reconfigurable RO structure is proposed in Refs. [10, 11]. First, the concept of inhomogeneous structure is over-viewed in this section. Then, the schematic and operation of the topology-reconfigurable RO are explained.

A. Inhomogeneous RO Structure

In a conventional homogeneous RO structure, where all the inverting stages have the same structure, the oscillation period is a function of the delays of all the stages. Thus, delay variation of a particular stage cannot be measured. However, if the RO has a topology where a certain stage have multiple times larger delay than the other stages, then the delay of that particular stage becomes visible to the RO frequency. This kind of structure is known as inhomogeneous structure [7]. Figure 1 shows an nMOSFET-sensitive inhomogeneous structure and Fig. 2 shows the sensitivity coefficients for each transistor. The two nMOSFETs in the inhomogeneous stage have more than 40 times higher sensitivities at 0.8 V operation. The

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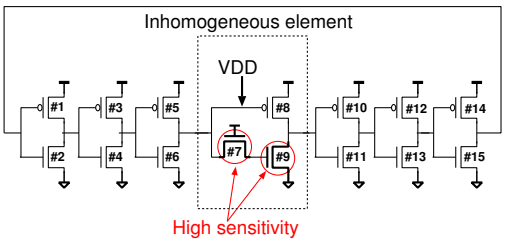

Fig. 1. An inhomogeneous RO structure for nMOSFET variability characterization.

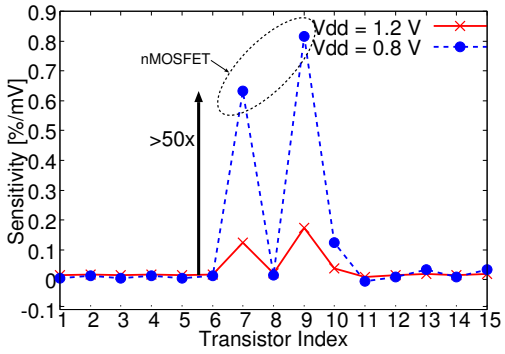

Fig. 2. Sensitivity of each transistor for RO frequency. nMOSFETs in the inhomogeneous stage have large sensitivity compare to others.

inhomogeneity has been created by operating the pull-down nMOSFET of the inhomogeneous stage at a reduced gate over-drive than the other MOSFETs. As MOSFET current depends strongly on the gate over-drive, the delay sensitivity becomes multiple times larger. Utilizing this feature, we show in Sec. III that delay characterization of individual gates is possible by making the RO structure reconfigurable where several pull-up and pull-down paths can be selected independently.

B. Topology-Reconfigurable RO Structure

Using the concept of the inhomogeneous structure, a topology-reconfigurable RO structure is proposed in Refs. [10, 11]. Figure 3(a) shows the schematic of the topology-reconfigurable RO and Fig. 3(b) shows the topology-reconfigurable inverter structure to achieve the reconfigurability. The RO structure of Fig. 3 can be configured into both homogeneous and inhomogeneous structures. Figures 3(c), 3(d) and 3(e) show three topology structures of the inverter cell. Figures 3(c) has the characteristics of a standard inverter cell. Figures 3(d) and 3(e) are nMOSFET-sensitive and pMOSFET-sensitive structures by which independent characterization of the two MOSFET types is performed. Next, by scanning the inhomogeneous stage, large number of samples can be obtained. By changing the topology inside the inhomogeneous stage, further enhancement in sample number as well as transistor-by-transistor visibility can be achieved. Utilizing the topology-reconfigurability inside the inhomogeneous structure, this paper proposes an parameter extraction method to extract individual transistor parameters.

The key feature of the topology-reconfigurable inverter

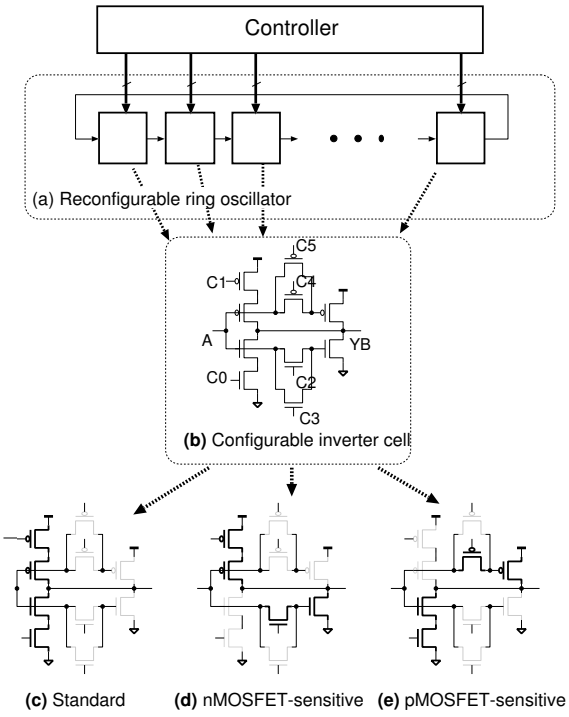

Fig. 3. Topology-reconfigurable monitor circuit for in-situ variability characterization.

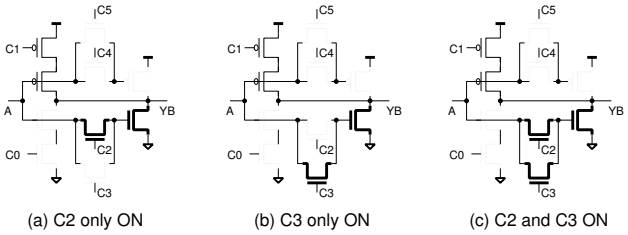

Fig. 4. Three different nMOSFET-sensitive configurations of topology-reconfigurable inverter.

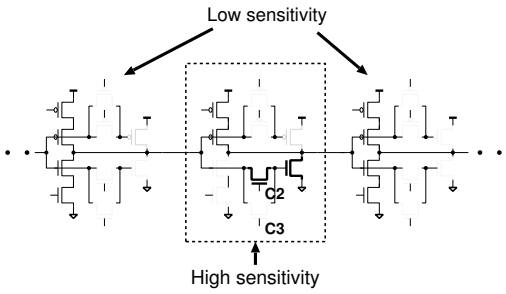

Fig. 5. An nMOSFET-sensitive inhomogeneous RO topology. The inhomogeneous stage delay sensitivity is multiple times larger than the other stages.

cell of Fig. 3(b) is that several pull-down or pull-up paths can be activated by configuration. For example, nMOSFET-sensitive topology can be achieved by three different topologies of Figs. 4(a), 4(b) and 4(c). The three configurations of the nMOSFET-sensitive structure have three nMOSFETs involved. The three nMOSFETs are the two pass-gates and the pull-down nMOSFET. Figure 5 shows an example of an nMOSFET-sensitive inhomogeneous RO topology. The inhomogeneous stage delay sensitivity is more than 40 times larger than the other stages at 0.8 V operation. Thus, the delay deviation between the prediction made by transistor level simulation and the measurement is a strong function of the inhomogeneous stage MOSFETs. As three frequency measurements for the three topologies shown in Fig. 4 are obtained, they can be expressed by the following linear approximations assuming threshold voltage to be the parameter of interest.

$$\Delta d_{\mathrm{n}1} = k_{\mathrm{n}1,1}\Delta V_{\mathrm{tn},1} + k_{\mathrm{n}3,1}\Delta V_{\mathrm{tn},3}, \quad (1)$$

$$\Delta d_{\mathrm{n}2} = k_{\mathrm{n}2,2}\Delta V_{\mathrm{tn},2} + k_{\mathrm{n}3,2}\Delta V_{\mathrm{tn},3}, \quad (2)$$

$$\Delta d_{\mathrm{n}3} = k_{\mathrm{n}1,3}\Delta V_{\mathrm{tn}1} + k_{\mathrm{n}2,3}\Delta V_{\mathrm{tn},2} + k_{\mathrm{n}3,3}\Delta V_{\mathrm{tn},3}. \quad (3)$$

Here, $\Delta d_{\mathrm{n},1}$, $\Delta d_{\mathrm{n},2}$ and $\Delta d_{\mathrm{n},3}$ are delay deviations for the three nMOSFET-sensitive inhomogeneous RO topologies. Delay deviation is the difference between the measurement and the prediction. $\Delta V_{\mathrm{tn},1}$ and $\Delta V_{\mathrm{tn},2}$ are threshold voltage variations for the two nMOSFET pass-gates. $\Delta V_{\mathrm{tn},3}$ is the threshold voltage variation for the pull-down nMOSFET. $k_{\mathrm{n}1,1}$ and $k_{\mathrm{n}3,1}$ are sensitivity coefficients for the 1st pass-gate and the pull-down nMOSFET for the Fig. 4(a). Transistor level simulation based on RC extracted netlist is performed to obtain the sensitivity coefficients. Similarly, equations for pMOSFET-sensitive topologies are obtained as follows.

$$\Delta d_{\mathrm{p}1} = k_{\mathrm{p}1,1}\Delta V_{\mathrm{tp},1} + k_{\mathrm{p}3,1}\Delta V_{\mathrm{tp},3}, \quad (4)$$

$$\Delta d_{\mathrm{p}2} = k_{\mathrm{p}2,2}\Delta V_{\mathrm{tp},2} + k_{\mathrm{p}3,2}\Delta V_{\mathrm{tp},3}, \quad (5)$$

$$\Delta d_{\mathrm{p}3} = k_{\mathrm{p}1,3}\Delta V_{\mathrm{tp}1} + k_{\mathrm{p}2,3}\Delta V_{\mathrm{tn},2} + k_{\mathrm{p}3,3}\Delta V_{\mathrm{tp},3}. \quad (6)$$

III. Proposed Characterization Methodology

We propose a methodology for in-situ variability characterization of individual transistors. First, the problem of sensitivity-based parameter estimation technique is described. Then, the proposed methodology is explained.

A. Sensitivity-based Estimation Technique

In a RO-based characterization, the RO frequency variation needs to be converted to the underlying parameter variations. This can be done by reverse calculating using sensitivity coefficients [4, 5, 7]. For example, in the case of RTN-induced delay fluctuation is converted to threshold voltage fluctuation using sensitivity coefficient. However, the sensitivity coefficient itself may contain error due to the variation as the delay sensitivity is largely affected by device performances. Conventionally, the sensitivity coefficients are calculated assuming the transistors are in the typical condition. However, the sensitivities fluctuate largely depending on the variability states of each transistor. One such example is shown in Fig. 6

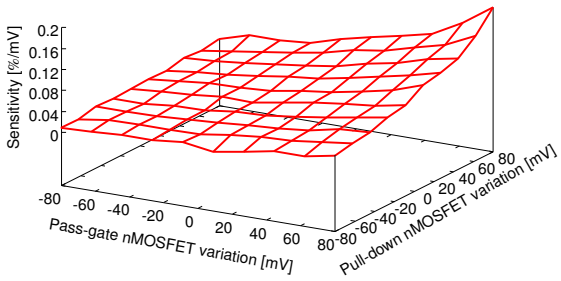

Fig. 6. Sensitivity of pass-gate nMOSFET 4(a) configuration against within-die variation of pass-gate and pull-down nMOSFETs.

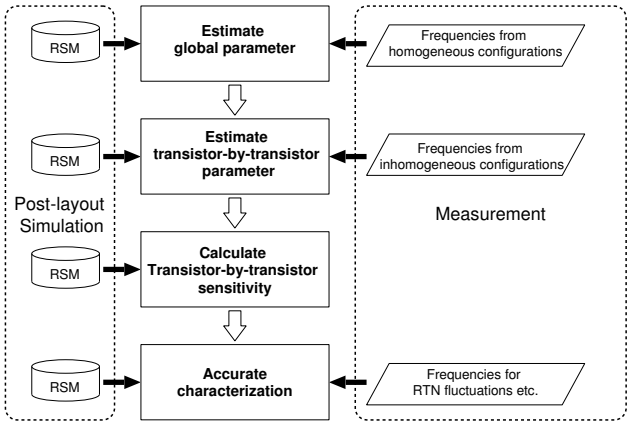

Fig. 7. Estimation flow of transistor-by-transistor parameter and sensitivity.

where the sensitivity of the nMOSFET pass-gate of Fig. 5 is plotted against the threshold voltage variation of itself and the pull-down nMOSFET. Multiple times of sensitivity fluctuation is being observed. Thus, it is important to consider global variation as well as each transistor's local variation during variability characterization.

B. Proposed Characterization Methodology

Figure 7 shows the overall estimation flow. First, the transistor model needs to be correlated with the target chip. This is achieved by estimating the global variations of nMOSFET and pMOSFET threshold voltages of the target chip using homogeneous configurations [5]. The estimated values of global variations are then fed into the transistor models. Then, frequencies are measured for each of the inhomogeneous RO topologies. These measurements provide the within-die or local delay variations between the stages. Using the updated transistor models, within-die variation for each transistor will be estimated using the Eqs. (1)∼(6). In order to characterize dynamic variations such as RTN, RO frequency is measured for a long time for each of the inhomogeneous topologies. sensitivity coefficients are then calculated incorporating each transistor's local variation. These sensitivity coefficients are then used to convert delay fluctuation to threshold voltage fluctuation which is an important parameter for RTN characterization.

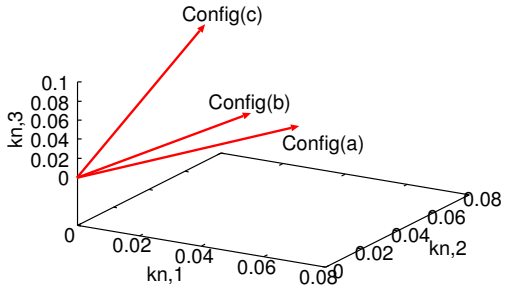

Fig. 8. Sensitivity vectors of RO frequencies to three nMOSFETs.

C. Transistor-by-transistor Local Variation Characterization

For the nMOSFET-sensitive inhomogeneous RO topologies, three equations of Eqs. (1) $\sim$ (3) can be achieved for each inhomogeneous stage. As the target parameters to be estimated are the threshold voltage variations of the three nMOSFETs, the parameters can be estimated by solving the following equation.

$$\vec{V_{\rm n}} = {\mathbf{S}_{\rm n}}^{-1}\Delta\vec{D}_{\rm n}, \tag{7}$$

Where,

$$\vec{V_{\rm n}} = \begin{pmatrix}\Delta V_{\rm tn1}\\ \Delta V_{\rm tn2}\\ \Delta V_{\rm tn3}\end{pmatrix}, \mathbf{S}_{\rm n} = \begin{pmatrix}k_{\rm n1,1} & k_{\rm n2,1} & k_{\rm n3,1}\\ k_{\rm n1,2} & k_{\rm n2,2} & k_{\rm n3,2}\\ k_{\rm n1,3} & k_{\rm n2,3} & k_{\rm n3,3}\end{pmatrix} \tag{8}$$

and

$$\Delta\vec{D}_{\rm n} = \begin{pmatrix}\Delta f_{\rm n1}\\ \Delta f_{\rm n2}\\ \Delta f_{\rm n3}\end{pmatrix}. \tag{9}$$

Here, $\vec{V_{\rm n}}$ is the vector for the three unknown threshold voltage variations. $\mathbf{S}_{\rm n}$ is the sensitivity matrix and $\Delta\vec{D}_{\rm n}$ is the measured delay variations for the three topologies. Successful extraction of threshold voltages of the three nMOSFETs depends on the sensitivity matrix $\mathbf{S}_{\rm n}$. Condition number is used to express the robustness of any matrix. Smaller the condition number, more robust the estimation becomes. The sensitivity matrix for the nMOSFET-sensitive topologies are shown below.

$$\mathbf{S}_{\rm n} = \begin{pmatrix}0.0715 & 0.0000 & 0.0927\\ 0.0000 & 0.0715 & 0.0927\\ 0.0355 & 0.0355 & 0.0536\end{pmatrix}. \tag{10}$$

The condition number of the matrix $\mathbf{S}_{\rm n}$ is calculated to be 10 which shows strong robustness against any uncertainties in the measurements. Figure 8 visualizes the sensitivity vectors to assure that accurate estimation is possible. Large angles are formed between the vectors. Similarly, the threshold voltage variations for the two pMOSFET pass-gates and the pull-up pMOSFET can be estimated.

IV. Measurement and Characterization Results

Measurements and characterizations of nMOSFET variations have been performed for a 65 nm test chip. In this section, test chip design and measurement procedures are described first. Then, measurement and characterization results are described.

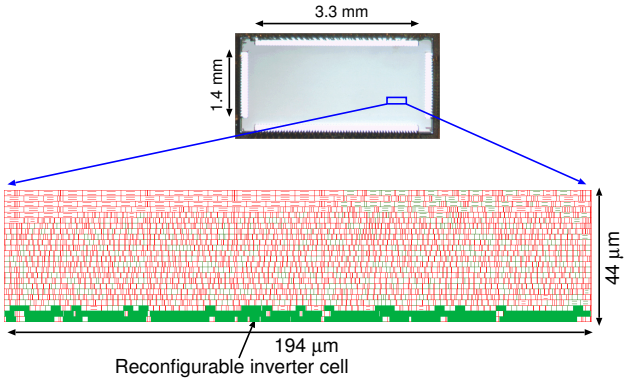

Fig. 9. Chip micrograph and monitor circuit layout.

A. Test Chip Design and Measurement Procedure

A test chip has been designed and fabricated in a 65 nm process to validate the proposed characterization methodology. Figure 9 shows the chip micrograph and the layout of our topology-reconfigurable RO along with decoders, dividers, and shift registers. The number of stage is set to 127. The first stage is an NAND gate to control the oscillation. The remaining 126 stages can be configured to various topologies as shown in Fig. 4. For example, for nMOSFET variability characterization, the RO is configured as an inhomogeneous structure where the inhomogeneous stage is configured to one of the three configurations of Fig. 4. Then, three frequencies are measured for the three configurations. Next, the inhomogeneous stage is swapped between the next stage, and three frequency measurements are performed. This way, by swapping and scanning the inhomogeneous stages, 126 sets of frequency measurements for nMOSFET characterization are achieved. Each set corresponds to the same inhomogeneous stage. In total, $126 \times 3 = 378$ frequency measurements are obtained for nMOSFET characterization. Frequency fluctuation has been measured over 22 s with an integration time of 1 ms for each of the inhomogeneous topologies for RTN characterization.

B. Measurement Results

Figures 10, 11 and 12 show the frequency distributions for the three nMOSFET-sensitive topologies as shown in Fig. 4 at 0.8 V supply voltage. All the frequencies are normalized by the mean value of Fig. 4(a) configuration. Tails are observed for the frequency distributions which results from the following two factors. One is the non-linear relationship between the RO frequency and transistor variation. The other is the effect of output interconnect capacitance. In this test chip, automatic place and route is performed which places the inverter cells to minimize the interconnect lengths. The effect of non-linearity can be overcome by applying an iterative estimation technique [5]. The effect of output capacitance can be overcome by either calculating sensitivity coefficients for each stage considering

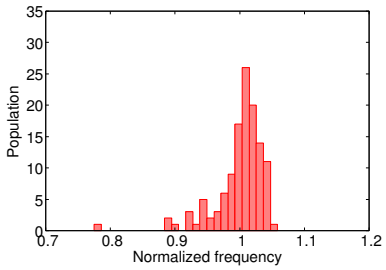

Fig. 10. Frequency distribution for nMOSFET-sensitive inhomogeneous configuration where Fig. 4(a) configuration is used in the inhomogeneous stages.

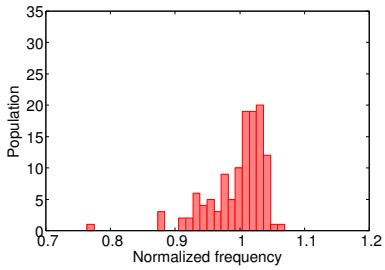

Fig. 11. Frequency distribution for nMOSFET-sensitive inhomogeneous configurations where Fig. 4(b) configuration is used in the inhomogeneous stages.

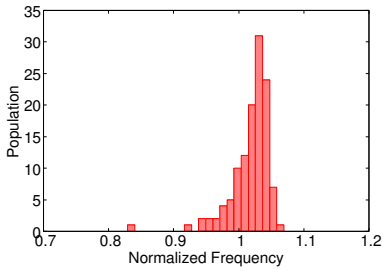

Fig. 12. Frequency distribution for nMOSFET-sensitive inhomogeneous configurations where Fig. 4(c) configuration is used in the inhomogeneous stages.

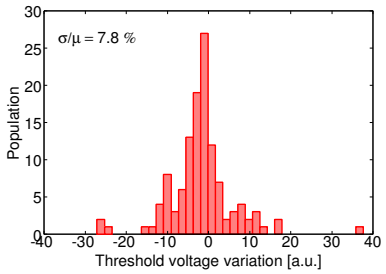

Fig. 13. Distribution of threshold voltage variation for nMOSFET pass-gate 1.

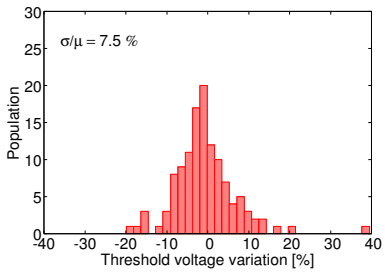

Fig. 14. Distribution of threshold voltage variation for nMOSFET pass-gate 2.

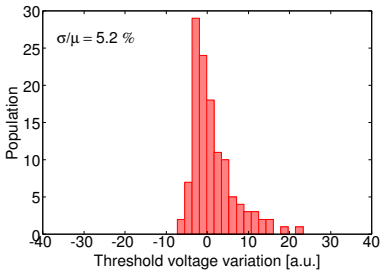

Fig. 15. Distribution of threshold voltage variation for pull-down nMOSFET.

its output capacitance, or placing the cells adjacent to each other to make sure that all the stages have similar load capacitance. However, the main point is from the three frequency measurements, linear equations of Eqs. (1), (2), and (3) can be built for each of the stages. Next, these three equations are solved to obtain threshold voltage variations for the two nMOSFET pass-gates and the pull-down nMOSFET.

C. Characterization of Individual Transistor Variation

First, global variations of nMOSFET and pMOSFET are estimated for the target chip. Then, threshold voltage variations for the three nMOSFETs are estimated using Eq. (7). Figures 13 $\sim$ 15 show the estimated threshold voltage variations for the two nMOSFET pass-gates and the pull-down nMOSFET. The estimated $\sigma_{V_{\rm tn}}/\mu_{V_{\rm tn}}$ of the two pass-gates are 7.8 % and 7.5 %. Here, a fixed value of $\mu_{V_{\rm tn}}$ is assumed for the pass-gates as well as the pull-down nMOSFET. The two pass-gates have identical layout, thus similar variation between the pass-gates suggests that the estimation framework has worked correctly. Figure 15 shows tail in the distribution which is the result of non-linearity of RO frequency to the variations. Load capacitance variation may also effect the estimation. The use of multiple iteration and consideration of output load capacitance remain in our future work. The $\sigma_{V_{\rm tn}}/\mu_{V_{\rm tn}}$ value of the pull-down nMOSFET is calculated to be 5.2 % which is much smaller than those of the pass-gates. The pass-gates receive strong reverse body bias as the source voltages of the pass-gates increase. As a result, the pass-gates have higher threshold voltages, and thus spreader distribution is expected for the pass-gates. Smaller variation for the pull-down nMOSFET which is not affected by body bias suggests the correctness of the estimation methodology.

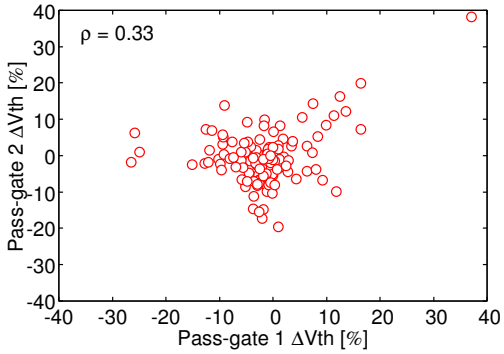

Fig. 16. Correlation between estimated threshold voltages of nMOSFET pass-gates. Correlation coefficient, ρ, is 0.33.

Next, we show the correlation between the estimated threshold voltage variations for the two pass-gates in Fig. 16. No clear correlation has been observed for the estimations which confirms the robustness of the estimation methodology.

D. Characterization of RTN

Figure 17 shows the CDF (Cumulative Distribution Function) of frequency fluctuation for the two topologies of fig. 4(a) and 4(b) topologies. Long tail is being observed which is a characteristic of RTN. Frequency fluctuation of Fig. 17 is then

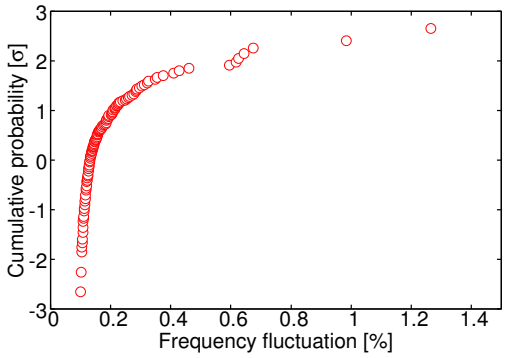

Fig. 17. CDF of RTN induced frequency fluctuation for nMOSFET-sensitive inhomogeneous configuration.

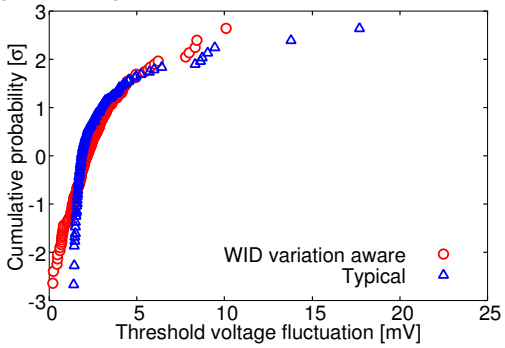

Fig. 18. CDF of RTN induced threshold voltage fluctuation for nMOSFET.

converted into threshold voltage fluctuation using sensitivity coefficients of the pull-down nMOSFET. Figure 18 plots the CDF of threshold voltage fluctuations. The triangular points represent the calculated threshold voltage fluctuations without considering each transistor's variability. Maximum of 19 mV of threshold voltage fluctuation is observed in this case. The circle points represent the calculated threshold voltage fluctuations when sensitivity based on each transistor's variation is used for the calculation. The maximum fluctuation is reduced to 13 mV. The shapes of the two CDFs differ suggesting if local variation is not considered the characterization may contain large error especially at higher σ levels.

V. Conclusion

In-situ variability characterization methodology of individual transistors has been proposed using a topology-reconfigurable RO structure. Utilizing the topology-reconfiguralability, variations of individual transistors are estimated using linear equations. A test chip containing a topology-reconfigurable RO has been fabricated in a 65 nm process. Estimation of local threshold voltage variations for each transistor has been performed successfully. Then, RTN-induced threshold voltage fluctuation has been characterized considering individual transistor's variability. Thus, transistor level variability characterization gives us accurate information and more visibility on the interactions of the various variation types. The proposed method can be used for accurate characterization of die-to-die, within-die, RTN and NBTI variations.

Acknowledgments

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