2012 IEEE 21st Asian Test Symposium

On-chip Detection of Process Shift and Process Spread for Silicon Debugging and Model-Hardware Correlation

Islam A.K.M Mahfuzul*, Hidetoshi Onodera*‡
* Graduate School of Informatics, Kyoto University, Kyoto, Japan
‡ JST, CREST
email: {mahfuz,onodera}@vlsi.kuee.kyoto-u.ac.jp

***Abstract*—This paper proposes the use of ROs (Ring Oscillators) for process shift and process spread detection for silicon debugging and model-hardware correlation. ROs are designed to be sensitive to either nMOSFET or pMOSFET variation, thus the location of the chip in the process space can be detected directly from the RO measurements. Test chip measurements in a 65-nm process shows the validity of the proposed ROs. Amounts of process shift and process spread for key process parameters as threshold voltages and gate length are extracted from test chip measurements.**

I. Introduction

Delay testing of manufactured IC in the nanometer process has become a very difficult task. Often the testing cost surpasses the manufacturing cost. Delay testing is performed to make sure that the product chip operates at the desired target operating frequency. However, due to process variation and other manufacturing faults, some parts may not achieve the desired frequency, and therefore delays of all the paths must be tested before shipping the product. When some parts of the chip do not achieve the desired frequency, the biggest challenge is to debug the causes of delay defect or timing failure. In case of delay defects, there are mainly two reasons. One is the parametric variation which is often called as process variation and the other is random defect [1].

Normally, process variation is used to express both process shift and process spread effects. Process shift refers to the shifts of several process parameters from target values. Process spread is the amount of variation within a chip. Process spread can be systematic or random. As Process shifts occur at the chip level or at the wafer level, they affect the gate delays globally and normally accounted by considering their effects in the transistor models. Usually, several extreme cases are modeled which are called the corner models. Designers verify their design with the corner models. Typically, products's operating frequency is chosen to achieve maximum economic benefit. For the designers, there are two options while selecting the operating frequency. One is to over design the circuits so that it will operate even at the worst-case process variation. However, under the ever increasing process variation in the scaled technology, worst-case design is way too inefficient to accept in today's high competitive market. Another option is to design the circuit for a typical process variation case, and categorize the products base on the performance such as speed binning [2]. Monitor circuits capable of quick detection of process variation and a low cost model-hardware correlation methodology is required.

In order to deal with process spread, several statistical design methods have emerged in recent years using the statistical nature of process spread. STA (static timing analysis) with OCV (on-chip variation) and SSTA (statistical STA) are two methods which use statistical nature of process variation and try to reduce the extra margins caused by simple STA [3]. STA with OCV is now being used in commercial tools for guard banding the effect of process spread on gate delays. In both the cases, on-chip monitoring of process shift as well as process spread has become more important for successful SSTA.

Monitoring of process shift and process spread is extremely costly. Generally, PCM (Process Control Module) and monitoring circuits are placed at the scribe lines to monitor process variation. However, they are not useful to debug the causes of timing failures. In order get information from the actual product chips, ring oscillators consisting of standard inverter or nand gates can be used to screen delay defects [4]. The frequencies of these monitor structures give us useful information on the process variation to some extent. However, we cannot get any information of process shift or process spread especially when the process shifts to slow pMOSFET and fast nMOSFET, or vice versa. When pMOSFET and nMOSFET move to opposite directions, maximum operating frequency of digital circuit does not correlate to ring oscillator frequency because the set of critical paths changes depending on the process variation. Especially for SRAM yield debugging, the location of the chip in the process space is an essential information that need to be monitored efficiently. This paper proposes two types of ring oscillators which is sensitive to either pMOSFET or nMOSFET variation only. From their frequencies process shifts in the chips can be detected directly. From frequencies obtained from the distributed RO instances spread over the chip, process spread for pMOSFET and nMOSFET using the proposed sensitized ROs can also be obtained.

The main contributions of this paper are as follows.

1) Detect process shift and process spread directly from process-sensitive ring oscillators.

1081-7735/12 $26.00 © 2012 IEEE
DOI 10.1109/ATS.2012.66

2) An efficient model-hardware correlation methodology is presented.

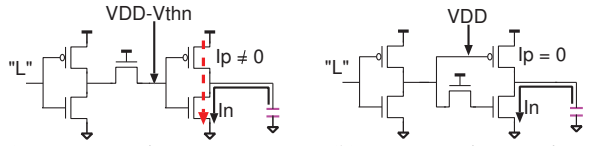
The proposed structures can be used to generate test pattern for exercising potential critical paths in the design because potential critical paths vary from corner to corner. Especially, when the process shifts, the proposed structure will provide direct information on the amount of that shift.

The following of the paper is organized as follows. In Sec. II, new pass-gate based inverter structures are proposed. The validity of using ROs consisting of the proposed inverter structures for detection of process shift and process spread is demonstrated here. Sec. III shows a test chip structure to measure and validate the proposed ROs. Sec. IV shows detailed measurement results from chips obtained from several process corners. In Sec. V, a methodology is presented to correlate model to silicon. Finally, Sec. VI concludes the paper.

II. Ring Oscillators for Process Shift and Process Spread Detection

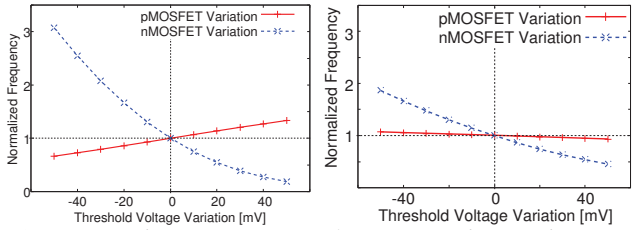
Conventionally, ring oscillators (RO) consisting of standard inverter cells are used as process monitors. These ROs give us useful information on the process. However, one disadvantage of using such ROs is that when the process moves to "SF" (slow nMOSFET and fast pMOSFET) or "FS" (fast nMOSFET and slow pMOSFET), the difference cannot be distinguished. These mismatch between nMOSFET and pMOSFET may cause unexpected timing failures. Besides, SRAM yield largely depends on the global and local mismatches between nMOSFET and pMOSFET. Thus, monitoring global variation as well as local random variation is necessary for yield optimization and silicon debugging. In order to debug the causes of the defects, monitor circuits capable of detecting the location of product chip in the process space and the amount of process spread are required. On-chip monitor circuits which can be embedded on the product chips are required, because PCM data may not reflect the actual silicon condition of the product chips.

ROs consisting of modified inverter structures to capture various process information and data analysis techniques are proposed in recent years [5]–[7]. This paper is inspired by their work, and enhances their works by proposing the use of a set of monitor circuits by which quick detection of process shift and process spread is possible. The proposed monitors will give us instant insight on the parameter fluctuations. Furthermore, the proposed ROs can be used to correlate model-hardware behaviour and improve the product quality level.



(a) Pass transistor at output (b) Pass transistor at input

Fig. 1. Inverter with nMOSFET pass transistor at the input is sensitive to nMOSFET variation only.



(a) Pass transistor at output (b) Pass transistor at input

Fig. 2. Sensitivity to MOSFET threshold voltage variation. Structure of (b) is sensitive to particular MOSFET variation thus suitable for parameter extraction.

In order to detect process variations, RO frequency needs to be sensitized to the variation effects. In order to detect mismatch between nMOSFET and pMOSFET, ROs sensitive to either of the MOSFETs are required. The use of pass-gate based inverter structure for process characterization is proposed [5]. Fig. 1(a) shows the conventional pass-gate based inverter structure where the pass-gate is placed at the output of the inverter cell. nMOSFET pass-gate based structure increases the inverter delay sensitivity to nMOSFET parameter variations because pass-gate's delay depends on the threshold voltage directly. Although the Fig. 1(a) structure is extremely useful for the analysis of process variation, it has one problem to be used in the direct process monitoring. For pass-gate structure in Fig. 1(a), the output voltage of the pass-gate does not go fully high because of the voltage drop across the pass-gate. As a result, pMOSFET of the next stage is partially on during the pull down of the next stage. This make through current to flow during the pull down which causes delay, and the inverter delay becomes sensitive to pMOSFET variation also.

In order to overcome the above problem, a new pass-gate structure is proposed which is shown in Fig. 1(b). The idea here is to increase the sensitivity to either nMOSFET or pMOSFET variation only. In Fig. 1(b), the voltage drop across the nMOSFET pass-gate is applied to the gate of nMOSFET only. Thus, pMOSFET is unaffected from the voltage drop and no through current flows. Fig. 2 shows the change of RO frequency to MOSFET threshold variations for inverter structures of Fig. 1(a) and Fig. 1(b). Here, nMOSFET pass-gate based inverter structure is used. In Fig. 2(a), the conventional structure is sensitive to nMOSFET variation. However, the frequency also changes largely when pMOSFET threshold voltage varies. When pMOSFET threshold voltage lowers meaning pMOSFET becomes faster, the RO frequency decreases instead of increasing. This behaviour is the opposite to the behaviour found in conventional CMOS digital circuits. This is because when pMOSFET becomes faster, the through current increases resulting in large delay during the pull-down. So, RO consisting of this structure will not give us direct in-sight into the process variation. In Fig. 2(b), the RO frequency for the proposed inverter structure is not sensitive to pMOSFET variation. The frequency is sensitive to nMOSFET variation thus suitable for process shift and process spread

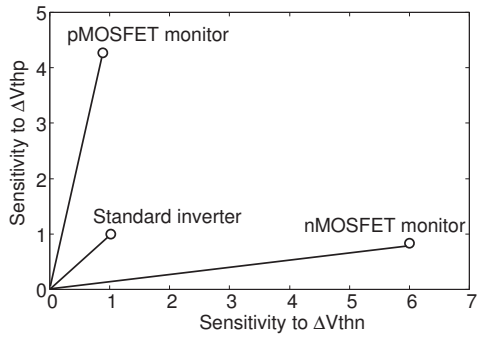
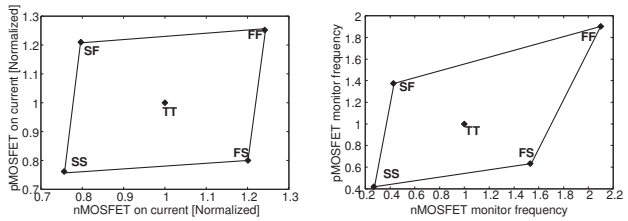


Fig. 3. Sensitivity vectors of proposed process monitors and RO with standard inverter cell. Vectors of the process monitors are near orthogonal, thus suitable for process corner detection.



(a) MOSFET on current (b) Proposed monitor frequency

Fig. 4. MOSFET on currents (a) and monitor frequencies (b) simulated at the process corners. Monitor frequencies are distributed in the process space.

detection.

Fig. 3 shows the sensitivity vectors of the proposed process monitors and an RO consisting of a standard inverter cell. X-axis and Y-axis refer to $\Delta V_{\rm thn}$ and $\Delta V_{\rm vthp}$ sensitivities respectively. The vector values are normalized with the sensitivity of the standard RO to nMOSFET threshold variation. Standard inverter based RO has similar sensitivities to nMOSFET and pMOSFET variations whereas proposed monitors are highly sensitive to either nMOSFET or pMOSFET variation.

Next, we show the capability of process corner detection comparing to the corner models. Fig. 4(a) shows the simulated MOSFET on currents for the process corners. The on currents at the corner models form a rectangular shape. The actual on currents in the silicon is expected to be within the corner boundary. Fig. 4(b) shows the monitor frequencies simulated for corner models. In Fig. 4(b), the frequencies form a boundary within which the actual silicon values are expected to be. The main point here is that "SF" and "FS" corners are clearly distinguishable from the frequencies of the proposed monitors.

Standard inverter cell RO can also be embedded in the product chips as a reference RO. From the measurements of nMOSFET and pMOSFET monitors, and standard inverter cell RO, the amount of shift and spread in the transistor model parameters can also be derived which will be shown in Sec. V for model-hardware correlation. Therefore, we propose to use our proposed monitors along with the standard inverter cell RO.

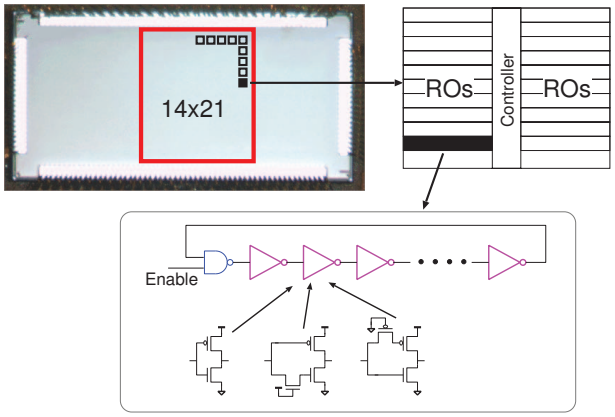


Fig. 5. Test chip structure. ROs consisting of the proposed inverter structure and the standard inverter structure are implemented.

III. Test Chip Design

A test chip in a 65-nm process has been designed to verify the monitor circuits use for process detection. Fig. 5 shows the chip micro-graph and overall structure of the test chip. 294 RO blocks are implemented with an array of 14×21. In real product chip, the ROs can be embedded into the chip at several various locations. Here the purpose is to make in-depth analysis and confirm the validity of the monitor circuits. Each block consists of our proposed monitor circuits and standard inverter cell RO. A decoder selects an RO and a selector selects the output of the oscillating RO. The output frequency is captured outside the chip. Dividers are used to reduce the frequency. Select signals are provided from outside the chip. All the ROs are 13-staged. The average value of frequencies of a RO type will give the information on process shift. Deviations in the frequencies will give us the information on process spread.

IV. Measurement Results

The ability of the proposed monitors to detect process shift and process spread will be demonstrated here. Test chips have been fabricated targeting "TT" condition, as well as four corners of "SS", "FF", "FS" and "SF". 5 chips from each of the process corners are measured.

A. Global Variation (Process Shift)

Frequencies of nMOSFET monitor and pMOSFET monitor from all the corner chips are plotted in Fig. 6. Both WID variation and D2D variation are observed. The frequency values are normalized by the values estimated with the "TT" corner model. Frequency values estimated at other corner models are also plotted for comparison. In Fig. 6, the corners are distinguished with the monitored frequencies. In Fig. 6, corners in actual silicon and in the model are not matched completely. Clear deviations are observed for "TT", "SS", "SF" and FS" corners. From the measurements, the silicon values are higher than the model values. Thus, with comparison with the models, we can have quick understanding of the process variation and position of the chip in the process space. This

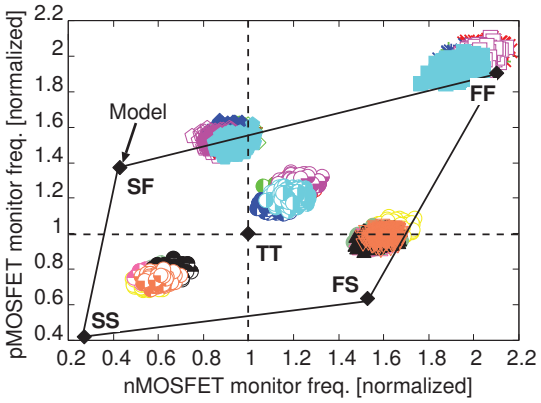


Fig. 6. Measured monitor frequencies from 5 chips per corner. Each chip contains 294 instances of each monitor.

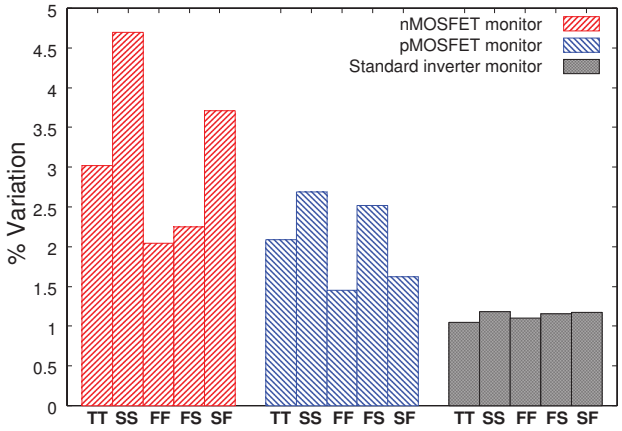


Fig. 7. WID variation observed in nMOSFET monitor, pMOSFET monitor and standard inverter ROs at the corner chips.

information will allow us to take decisions for silicon debug and test pattern generation. By doing further analysis, model-hardware correlation can also be performed which will allow us to tune the designs. Model-hardware correlation results will be presented in Sec. V.

B. WID Variation (Process Spread)

WID variation plays a major role in determining SRAM yield. For accurate SSTA, the WID variation needs to be monitored periodically to ensure product quality. As the ROs are very small in area, multiple instances of them can be spread over the chip. The measurements of all the RO instances will give valuable information on WID variation as well.

In our test chip, we have 294 instances of the same RO type embedded on the chip. WID variations of our proposed monitors and standard inverter ROs are calculated. The results are shown in Fig. 7. From standard inverter RO measurements, similar WID variation is observed for all the corner chips. However, for the nMOSFET monitor and pMOSFET monitor, significant differences in WID variation between the corner chips are observed. In "FS" corner, nMOSFET monitor's variability becomes smaller and pMOSFET monitor's variability becomes larger than their "TT" corner values. This indicates that the intrinsic variability in the nMOSFET and pMOSFET performances are different in the unbalanced corners which may cause the yield to decrease drastically [8]. The extend of the WID variation needs to be accurately monitored and feedback into the design. Our monitors are suitable for distinguishing nMOSFET and pMOSFET variations. In order to model the effects of WID variations, the variation needs to be expressed by transistor model parameters so that designers can use them. In Sec. V, obtained WID variation will be decomposed and modeled into variations of three transistor model parameters of threshold voltages and gate length.

V. Model-Hardware Correlation

A. Global Variation

After detecting the process shift of the product chips, the next step is to correlate those shifts to the model parameters. Model-hardware correlation is a time consuming process and normally performed from the I–V measurements of MOSFETs. PCM (Process Control Module) data provides us key transistor parameters (threshold voltage, on and off currents) by which we can modify the models. PCM module is located separated from the product chips and often they are single MOSFET which may not reflect the actual deviation inside the product chip. Besides, PCM data show the DC characteristics which may not reflect the variation observed in the digital circuits. In order to overcome these problems, RO frequency data from the product chips are preferable to detect the variation and feed the variation into the model.

Ref. [9] shows a methodology to decompose RO frequencies into several key process parameters such as threshold voltages and gate length. The proposed monitor circuits along with the standard inverter RO can be embedded into the product chip for the extraction of parameter deviation from the measured frequencies. In this test chip, we have extracted $\Delta V_{\rm thn}$, $\Delta V_{\rm thp}$ and ΔL against in the "TT" corner model for all the chips using the method described in [9]. In the extraction, $\Delta V_{\rm th}$ is expressed by the transistor model parameter "delvt0" which is a dedicated parameter for modeling threshold voltage shift in HSPICE. The values are shown in table I. Here, negative values of threshold voltage deviation refers that the absolute value is lower than that in the "TT" model.One key characteristics derived from the real chip measurement is that the gate length does not vary much compare to the variations in the threshold voltages. Large threshold voltage shifts are observed for the "FF" corner chip. This information can be incorporated into model and more efficient designs can be achieved.

Fig. 8 shows the threshold voltage corner in the model and the estimated corner from the RO frequencies. Threshold voltage values from the PCM data of "TT" corner wafer is also plotted. Estimated threshold voltages for "TT" corner chips are within the PCM data range but with some deviation from "TT" corner model. Large deviation is observed in threshold voltage values between estimation and model for "SS", "FS" and "SF" corners. In order to maintain high product quality

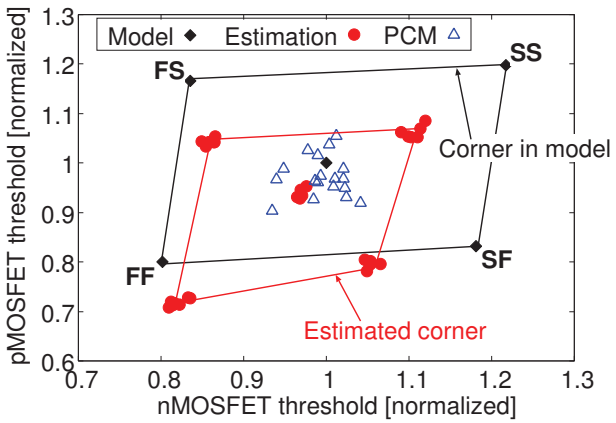


Fig. 8. Comparison between threshold voltage corners defined in transistor model and measured by monitor circuits.

Table I
ESTIMATION PARAMETER DEVIATION USING THE MONITOR CIRCUIT MEASUREMENTS AGAINST THE TYPICAL MODEL PARAMETER VALUES.

Corner	delvt0 [mV]		ΔL [nm]
	nMOSFET	pMOSFET	
TT	15.1	− 29.3	−0.38
SS	70.7	57.7	−2.1
FF	−111	−164	2.5
FS	−67.2	47.8	−3.2
SF	14.4	−122	3.2

and efficient design, transistor corner models can be updated with the estimated values.

B. WID Variation

If we put several instances of nMOSFET monitor, pMOSFET and standard inverter cell RO on the chip, then standard deviations can be derived for the RO frequencies assuming that random variation is the most dominant component in the WID variation. Next, we can extract the amount of variations in threshold voltages and gate length from the RO frequency variations by comparing with the simulation results. A method to extract parameter variations from process-sensitive RO frequencies is proposed in [10]. Using this method, the standard deviation of $V_{\rm thp}$, $V_{\rm thn}$ and L are derived from the measured standard deviations of each RO which is shown in Fig. 7. Derived values are shown in table II.

In table II, some interesting phenomena are observed. The amounts of standard deviations for $V_{\rm thp}$, $V_{\rm thn}$ and L are same for "FS" and "SF" corners. In case of L variation, the sigma value is larger in "FF" corner and smaller in "SS" corner. In case of threshold voltage variation, the sigma values are larger both in the "SS" and "FF" corners compare to the values in the "TT" corner. These information are extremely useful for SSTA and STA with OCV like statistical designs.

VI. CONCLUSION

This paper proposes the use of on-chip monitor circuits for detection of process shift and process spread for silicon debug, process characterization and model-hardware correlation. Special inverter structures are developed to make the ring oscillator frequency sensitive to either nMOSFET or pMOSFET variation. The proposed monitors along with the standard inverter RO embedded in the product chips, enable quick detection of process shift and process spread in the transistor model parameters such as threshold voltage and gate length. Extraction techniques for model-hardware correlation are presented. Global and WID variations in key transistor model parameters are successfully derived from chip measurements for several process corners designed in a 65-nm process.

Table II
EXTRACTED STANDARD DEVIATION OF MOSFET THRESHOLD VOLTAGES AND GATE LENGTH FROM RO FREQUENCY MEASUREMENTS.

Corner	$\sigma_{V_{\rm thn}}$ [mV]	$\sigma_{V_{\rm thp}}$ [mV]	σ_L [nm]
TT	16.6	11.9	0.89
SS	18.3	14.5	0.53
FF	20.9	16.6	1.14
FS	18.2	13.3	0.99
SF	18.2	13.6	0.99

ACKNOWLEDGMENTS

The authors would like to thank assistant professor Akira Tsuchiya for his lab support. Islam A.K.M Mahfuzul would like to thank lab member Shinichi Nishizawa for his support during the test chip design and measurement. The VLSI chip in this study has been fabricated in the chip fabrication program of VDEC, the University of Tokyo in collaboration with STARC, e-Shuttle, Inc., and Fujitsu Ltd.

REFERENCES

[1] S. Mitra and P. Ryan, "Delay defect characteristics and testing strategies," *IEEE Design & Test of Computers*, vol. 20, no. 5, pp. 8–16, Sep. 2003.

[2] a. Datta, S. Bhunia, S. Mukhopadhyay, and K. Roy, "Speed binning aware design methodology to improve profit under parameter variations," in *Asia and South Pacific Design Automation Conference*, 2006, pp. 712–717.

[3] a. Nardi, E. Tuncer, S. Naidu, A. Antonau, S. Gradinaru, T. Lin, and J. Song, "Use of Statistical Timing Analysis on Real Designs," in *Design, Automation & Test in Europe Conference*. Ieee, Apr. 2007, pp. 1–6.

[4] S. Mitra, E. Volkerink, E. McCluskey, and S. Eichenberger, "Delay defect screening using process monitor structures," in *Proceedings of 22nd IEEE VLSI Test Symposium*, no. Vts, 2004, pp. 43–48.

[5] M. Ketchen, M. B. and Bhushan, "Product-representative '' at speed '' test structures for CMOS characterization," *IBM Journal of Research and Development*, vol. 50, no. 4, pp. 451–468, 2006.

[6] A. Gattiker, M. Bhushan, and M. B. Ketchen, "Data analysis techniques for CMOS technology characterization and product impact assessment," in *IEEE International Test Conference*, 2006, pp. 1–10.

[7] V. Zolotov, D. Lackey, P. Ha, and C. Visweswariah, "Variation-aware performance verification using at-speed structural test and statistical timing," in *IEEE/ACM International Conference on Computer-Aided Design*, Nov. 2007, pp. 405–412.

[8] M. Yamaoka and H. Onodera, "A Detailed Vth-Variation Analysis for Sub-100-nm Embedded SRAM Design," in *IEEE International SOC Conference*, Sep. 2006, pp. 315–318.

[9] I. Mahfuzul, A. Tsuchiya, K. Kobayashi, and H. Onodera, "Variation-sensitive monitor circuits for estimation of Die-to-Die process variation," in *IEEE Intl. Conference on Microelectronic Test Structures*, 2011, pp. 153–157.

[10] S. Fujimoto, I. A. Mahfuzul, T. Matsumoto, and H. Onodera, "Inhomogeneous Ring Oscillator for WID Variability and RTN Characterization," in *IEEE Intl. Conference on Microelectronic Test Structures*, 2012, pp. 25–30.