Wide-Supply-Range All-Digital Leakage Variation Sensor for On-chip Process and Temperature Monitoring

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***Abstract*—Variation in process, voltage and temperature is a major obstacle in achieving energy-efficient operation of LSI. This paper proposes an all-digital on-chip circuit to monitor leakage current variations of both of the nMOSFET and pMOSFET independently. As leakage current is highly sensitive to threshold voltage and temperature, the circuit is suitable for tracking process and temperature. The circuit uses reconfigurable inhomogeneity to obtain statistical properties from a single monitor instance. An estimation method of threshold voltage variation is then developed. Cell-base design approach is taken so that design cost is minimized. Measurement results from a 65-nm test chip show the validity of the proposed circuit. Total area is 4500 μm^2 and active power consumption is 50 nW at 1.0 V operation. The proposed technique enables area-efficient and low-cost implementation thus can be used in product chips for applications such as testing and post-silicon tuning.**

I. Introduction

With device scaling, WID (Within-Die) random variation of transistor performance has been increasing resulting in large delay and leakage variation [1]. Energy loss due to leakage current has become a significant portion of the total energy consumption. It is therefore important to estimate leakage current of the target circuit during the design phase, as well as reducing leakage current by various post-silicon techniques, such as back-gate biasing, power gating etc. Thus, there is a strong need for on-chip leakage variation sensors that can be integrated and operated under wide supply operation.

Previously, analog approaches for leakage current sensing have been reported [2]. The analog approach has some limitations that the design is tuned for a particular supply voltage operation. Extra bias sources are required and different sensors are required for monitoring nMOSFET and pMOSFET independently. This paper proposes an all-digital leakage sensor circuit which has the ability to monitor leakage current of multiple devices from the same circuit instance. nMOSFET and pMOSFET leakage current variation can be monitored independently. The all-digital nature has been realized by using an ring oscillator (RO) structure where a particular node inside the RO is driven by leakage current. Inhomogeneous structure of RO is utilized so that delay due to leakage current is dominant in the oscillation period. Implementing reconfigurable inhomogeneous structure, multiple measurements are performed on the same circuit instance enabling independent statistical evaluation of nMOSFET and pMOSFET.

A reconfigurable inverter structure is developed to convert leakage current to delay in our leakage sensor. As the output of the monitor circuit is the RO frequency, digital measurement and process becomes possible. The proposed leakage variation sensor has the following characteristics. a) Digital, b) Wide-supply-range operation down to 0.5 V, and c) Monitor leakage variation for both of the nMOSFET and pMOSFET. The additional benefit that a leakage sensor provides is the ability to monitor temperature as well. As thermal management has become an integral part of most SoCs, temperature monitoring based on leakage sensor can be easily implemented on-chip [3]. We also propose an estimation method of threshold voltage variation from the monitored leakage variation. This makes the proposed monitor circuit an on-chip PCM (Process Control Module) which can be used to track process characteristics.

The remainder of the paper is organized as follows. In Sec. II, the concept of the proposed leakage variation sensing and the design of the reconfigurable leakage current monitor cell are described. In Sec. III, measurement results from a 65 nm process test chip are demonstrated to validate our circuit. Finally, Sec. IV concludes this paper.

II. All-digital Leakage Variation Sensor

A. Time-domain Leakage Current Monitoring

Leakage current needs to be converted to time-domain parameter such as delay to realize digital leakage current sensor. A technique to use MOSFET leakage current to pull-down or pull-up a capacitance node is used to develop a digital temperature sensor [3]. Figure 1 shows this concept by comparing operations of two inverter structures. In Fig. 1(a), a conventional inverter structure is shown where pull-up and pull-down MOSFETs are turned ON and OFF alternately depending on the input. The output node is charged and discharged by the ON currents. However, in Fig. 1(b), only the pull-up pMOSFET's gate is connected to the input and the pull-down nMOSFET's gate is tied down to "L". When the input is "L", the output node will be charged by the pMOSFET ON current. When the input is "H", both the MOSFETs turn OFF and only leakage currents exist. If the nMOFSET leakage current can be made multiple times larger than the pMOSFET leakage current, then the output node will be discharged by the nMOSFET leakage current. Similarly, pMOSFET leakage current can be converted to delay.

The delay characteristic is explained next by taking the example of discharging a node by nMOSFET leakage current. nMOSFET leakage current can be expressed by Eq. (1) when $V_{\rm ds}$ is much higher than the thermal voltage [4].

$$I_0 = I_{\rm ds0} e^{\frac{-V_{\rm th}+\lambda V_{\rm ds}-\gamma V_{\rm sb}}{nv_T}}, \quad (1)$$

$$I_{\rm ds0} = \beta v_T^2 e^{1.8}, \quad \beta = \mu C_{\rm ox}\frac{W}{L}. \quad (2)$$

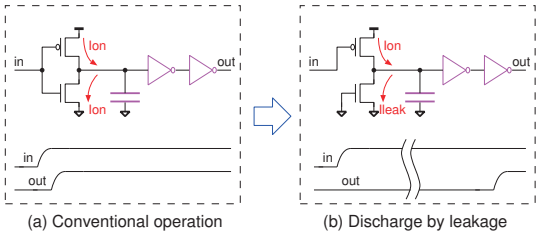

Fig. 1: Concept of converting leakage current to delay.

Here, μ is mobility, $C_{\rm ox}$ is gate capacitance, W is gate width, L is gate length, v_T is thermal voltage, n is subthreshold swing coefficient, λ is DIBL coefficient, and γ is body effect coefficient.

If the capacitance, $C_{\rm L}$, is discharged from $V_{\rm dd}$ to $V_{\rm inv}$ by nMOSFET leakage current, then

$$C_{\rm L}\frac{dV}{dt} + I_0(t) = 0, \tag{3}$$

$$C_{\rm L}e^{\frac{\lambda V}{nv_T}}dV = -I_{\rm ds0}e^{\frac{-V_{\rm thn}}{nv_T}}dt. \tag{4}$$

Here, $V_{\rm dd}$ is the supply voltage and $V_{\rm inv}$ is the logic threshold of the next inverter. Considering $V_{\rm sb}$ to be zero, the fall delay, $T_{\rm fall}$ is calculated by the following equation.

$$C_{\rm L}\int_{V_{\rm dd}}^{V_{\rm inv}} e^{\frac{\lambda V}{nv_T}}dV = -I_{\rm ds0}e^{\frac{-V_{\rm thn}}{nv_T}}\int_0^{T_{\rm fall}} dt \tag{5}$$

Solving the equation, we get

$$T_{\rm fall} = e^{1.8}\frac{nC_{\rm L}}{\lambda\beta v_T}e^{\frac{V_{\rm thn}}{nv_T}}\left(e^{\frac{-\lambda V_{\rm inv}}{nv_T}} - e^{\frac{-\lambda V_{\rm dd}}{nv_T}}\right). \tag{6}$$

By taking logarithm for both sides, we get

$$\log(T_{\rm fall}) = K_0 + \frac{V_{\rm thn}}{nv_T} + \log(e^{\frac{-\lambda V_{\rm inv}}{nv_T}} - e^{\frac{-\lambda V_{\rm dd}}{nv_T}}), \tag{7}$$

$$K_0 = 1.8 + \log(nC_{\rm L}) - \log(\lambda\beta v_T). \tag{8}$$

The delay have exponential relationship to $V_{\rm thn}$, thus can be used to monitor nMOSFET leakage current. Similarly, pMOSFET leakage current can be monitored.

B. Process Parameter Estimation from Leakage Variation

The variance of the logarithm of fall delay, $\log(T_{\rm fall})$, in Eq. (7) is calculated by

$$\sigma^2_{\log(T_{\rm fall})} = \frac{1}{(nv_T)^2}\sigma^2_{V_{\rm thn}} + \sigma^2_{\log(e^{\frac{-\lambda V_{\rm inv}}{nv_T}} - e^{\frac{-\lambda V_{\rm dd}}{nv_T}})}. \tag{9}$$

The second term in the equation corresponds to the logic threshold variation of the following inverter. Simulation results with a 65 nm transistor model confirm that the contribution of logic threshold variation to the delay variation is less than 3%. The amount of variation of logic threshold voltage can be reduced further by using larger transistors for the next inverter. Ignoring the logic threshold variation, the variation of the logarithm of the inverter delay becomes as follows.

$$\sigma_{\log(T_{\rm fall})} = \frac{1}{nv_T}\sigma_{V_{\rm thn}}, \tag{10}$$

$$\sigma_{V_{\rm thn}} = n \times v_T \times \sigma_{\log(T_{\rm fall})}. \tag{11}$$

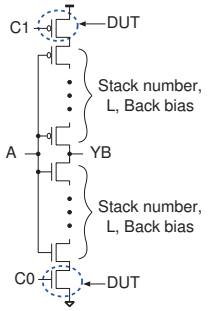

Fig. 2: Reconfigurable leakage monitor cell.

Table I: Configuration of leakage monitor cell.

Configuration ["C1","C0"]	Function
01	Standard inverter delay
00	nMOSFET leakage monitor
11	pMOSFET leakage monitor
10	Not used

As n and v_T are constant at a fixed temperature, $V_{\rm th}$ variation is calculated from delay variation with Eq. (11). Eq. (11) implies that the delay variation does not depend on supply voltage. Thus, wide-voltage-range operation can be achieved.

C. Topology-Reconfigurable Inverter Structure

Previously, we have proposed a topology-reconfigurable monitor circuit structure to monitor both of the D2D and WID variations from a single monitor instance [5]. In order to measure the leakage current variation, we use a similar topology-reconfigurable architecture. We have developed a topology-reconfigurable inverter structure to use in the circuit. Figure 2 shows the reconfigurable leakage monitor cell. Inverter in Fig. 2 has two configuration bits to turn ON or OFF the pull-down and the pull-up paths.

Next, we explain the operation of our leakage monitor cell for nMOSFET leakage monitoring. The C0 nMOSFET will be turned OFF and C1 pMOSFET will be turned ON. When the input is "L", the pull-up path turns ON and charges the output node. When the input is "H", both of the pull-up and pull-down paths turn OFF. However, all the stack pMOSFETs in the pull-up path turns OFF, whereas all except the DUT nMOSFET turns ON in the pull-down path. Leakage current reduces exponentially with the increase of stack number [6]. By using large stack numbers, the leakage current ratio can be tuned so that pull-down current becomes several times larger than spull-up leakage current. The output node is discharged gradually by the nMOSFET leakage current. As nMOSFET DUT is OFF and other stack nMOSFETs are ON, the DUT leakage current is the dominant component of the overall pull-down leakage current. The ratio between pull-down leakage and pull-up leakage is controlled by increasing the stack number or gate lengths of the stack MOSFETs. Back-gate bias can also be applied to the stacked MOSFETs to tune the leakage ratio.

D. All-digital Leakage Variation Sensor

Figure 3 shows the schematic of our all-digital leakage variation sensor circuit. The sensor circuit consists of a ring oscillator (RO), a decoder, a shift register and a divider.

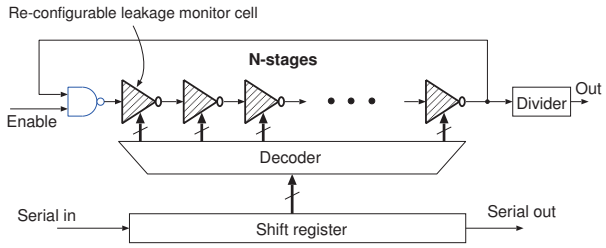

Fig. 3: Schematic of the reconfigurable leakage variation sensor circuit.

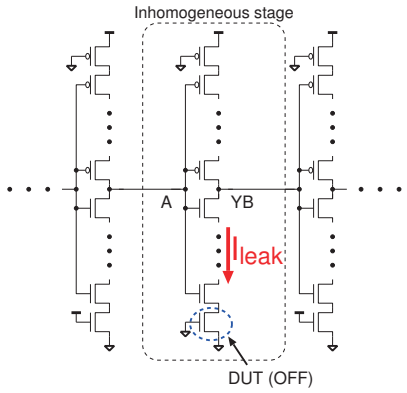

Fig. 4: Inhomogeneous structure to monitor single nMOFSET leakage current.

The oscillation frequency is counted outside the chip using a frequency counter. The ring oscillator consists of our developed topology-reconfigurable inverters as shown in Fig. 2. The number of stage, N, is 127. The configuration signals are set by the shift register. The decoder decides the control signals for each inverter stage. Each inverter stage can be controlled independently for realizing multiple configurations from a single circuit instance. The configuration modes for the reconfigurable monitor cells are summarized in Table I.

1) MOSFET Leakage Variation Measurement: MOSFET leakage variation is measured by configuring the RO as inhomogeneous and then measuring the oscillation period by swapping the inhomogeneous stage across the inverter chain [7]. Figure 4 shows an inhomogeneous configuration to monitor nMOSFET leakage current. The footer DUT nMOSFET in the inhomogeneous stage is turned OFF and footer nMOSFETs of other stages are turned ON. Thus, the discharge of the inhomogeneous stage will be driven by the nMOFSET leakage current. Similarly, pMOSFET leakage variation is measured by configuring the inverter as pMOSFET leakage sensor.

2) Average Leakage Measurement: Average leakage between the MOSFETs is measured by configuring the RO as homogeneous meaning all the inverter stages have the same configuration. Figure 5 shows a homogeneous configuration to monitor nMOSFET leakage.

3) Process Variation Estimation: The oscillation period of an inhomogeneous configuration is the sum of the delays for all the inverter stages, and is expressed with Eq. (12).

$$T = T_0 + Ke^{\frac{V_{\rm th}}{nv_T}}. \tag{12}$$

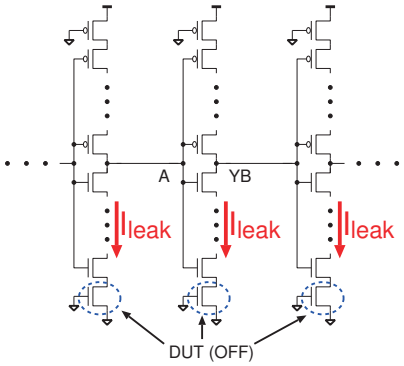

Fig. 5: Homogeneous structure to monitor average nMOSFET leakage current.

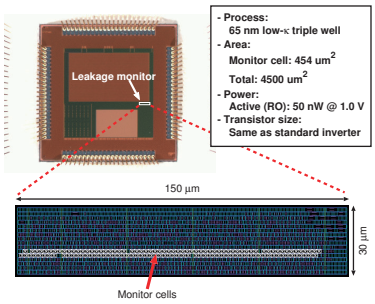

Fig. 6: Test chip micrograph and layout of the leakage variation sensor.

Here, T_0 is the delay component resulting from rise/fall delays driven by ON currents of the MOSFETs other than the DUT. K is constant here. T_0 is constant too from the fact that larger N average out random variation effect and that contribution of ON current delay is negligible compared with the leakage current delay. $T_{\rm osc}$ thus follows a log-normal distribution with three unknown parameters of the location, T, the mean, μ, the variance, σ^2. The probability distribution function is given as follows.

$$f_T(T;T_0,\mu,\sigma) = \frac{1}{(T-T_0)\sigma\sqrt{2\pi}} e^{\frac{-(\log(T-T_0)-\mu)^2}{2\sigma^2}}. \tag{13}$$

$V_{\rm th}$ variation is then expressed with the following equation.

$$\sigma_{V_{\rm th}} = n \times v_T \times \sigma_{\log(T-T_0)}. \tag{14}$$

III. Test Chip and Measurement Results

A. Test Chip Design

A test chip has been fabricated in a 65 nm process to validate our concept of leakage variation monitoring. Figure 6 shows the chip micrograph and the layout of the sensor circuit. A RO consisting of 126 inverting stages and a NAND gate is used to measure the delay variation. The pMOSFET gate width is 1.5 times larger than the nMOSFET gate width. Total area is 4500 μm^2. Active power during the oscillation is 50 nW at 1.0 V supply. Automatic place and route is performed with placement constraints applied to the monitor cells.

B. Measurement Results

1) Leakage Variation: Leakage variation is measured for both of the nMOSFET and pMOSFET by varying supply voltages to demonstrate the wide-supply-range operation. Figure 7

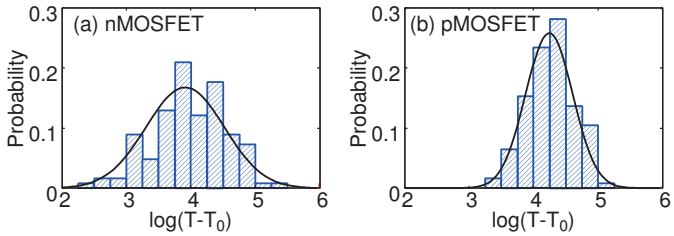

Fig. 7: Distribution of WID leakage variation. (a) nMOSFET, (b) pMOSFET. Log-normal distribution is observed.

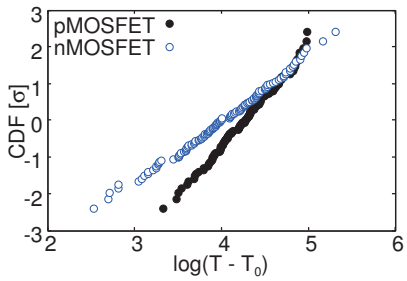

Fig. 8: CDF of WID leakage variation for nMOSFET and pMOSFET. The distribution fits log-normal distribution.

shows the delay distributions at 0.8 V supply for nMOSFET and pMOSFET after fitting the measured data to Eq. (13). The delay distributions follow log-normal distribution. This validates that the proposed monitoring technique is able to detect leakage variation. CDFs of the delay variations are shown in Fig. 8. In Fig. 8, nMOSFET has larger distribution than pMOSFET. Figure 9 shows the measured delay variation for different supply voltages. As Eq. (11) suggests, leakage variation does not depend on supply voltage. Measured variation is constant across wide range of supply voltages which validates our concept. $V_{\rm th}$ variation is then calculated from Eq. (11). nMOSFET $V_{\rm th}$ variation is 1.6 times larger than pMOSFET $V_{\rm th}$ variation which agrees with reported results obtained in 65 nm technology node [8], [9]. Thus, the proposed sensor monitors MOSFET leakage variation correctly.

2) Average Leakage Monitoring: When the monitor circuit is configured as a homogeneous structure, the total delay due to the N DUT MOSFETs' leakage current can be obtained. Figure 10 shows the oscillation periods for nMOSFET and pMOSFET measured at different supply voltage operation. Here, smaller the delay is, larger the leakage current is. In this particular chip, pMOSFET leakage is monitored larger than nMOSFET leakage. With the lowering of supply voltage, $V_{\rm th}$ increases because of DIBL effect. Measured oscillation

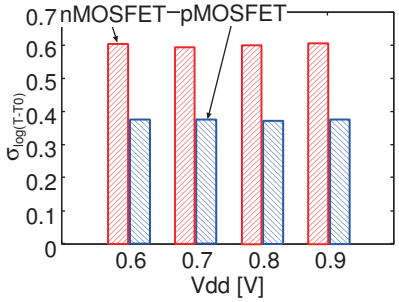

Fig. 9: Measured leakage variation at several supply voltage.

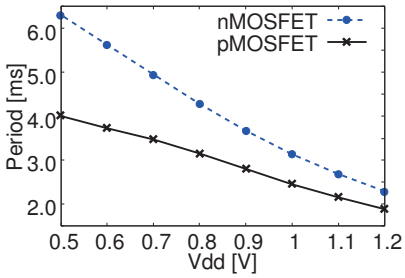

Fig. 10: Measured oscillation period due to N MOSFETs' leakage current at different supply voltages.

period shows the decrease of leakage current which shows that the capability of the circuit to track leakage variation.

IV. Conclusion

In this paper, we proposed a reconfigurable inverter cell which can be used as leakage current sensor. A RO based on-chip circuit is then developed to monitor WID leakage variation of nMOSFET and pMOSFET independently. Monitoring of leakage current variation gives us a deep insight into the process characteristics as well as enables temperature monitoring. Measurement results from a 65-nm test chip validate the proposed circuit. The sensor circuit is thus useful for on-chip monitoring of process and temperature, thus can be used for post-silicon tuning of MOSFET performances.

Acknowledgments

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