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A Built-in Self-adjustment Scheme with Adaptive Body Bias using P/N-sensitive Digital Monitor Circuits

Islam A.K.M Mahfuzul*, Norihiro Kamae*, Tohru Ishihara*, and Hidetoshi Onodera*†
* Graduate School of Informatics, Kyoto University, Kyoto, Japan
† JST, CREST
email: {mahfuz,kamae,ishihara,onodera}@vlsi.kuee.kyoto-u.ac.jp

***Abstract*—This paper proposes a built-in self-adjustment scheme to adjust pMOSFET and nMOSFET performances to their target values. Independent control of MOSFET performances can boost circuit performance without large leakage overhead. All-digital monitor circuits have been developed to detect pMOSFET and nMOSFET variations. The scheme has been fabricated in a 65 nm process. Measurement results from corner chips confirm the validity of the scheme. At 0.7 V operation, more than 50% of circuit speed degradation has been recovered. The proposed scheme achieves 2.6 times leakage saving than the conventional critical path delay based scheme. The scheme is suitable for typical-case design and yield enhancement.**

I. Introduction

Process variation has become a major concern in the scaled technology. Worst-case design is being used where significant amount of delay, power and area overheads are compromised. At lower supply operation, these overheads become way too high to accept as the variation effects are amplified by a multiple times [1]. Process variation causes unbalanced P/N-ratio resulting in larger delay. This delay increase is severe at near-threshold and sub-threshold operation. Adaptive body bias can be used to compensate P/N variations independently. Monitoring P/N variations becomes the key challenge here.

Critical path delay or MOSFET performance can be monitored to detect performance variation [2]–[4]. Body bias based compensation techniques are proposed where delay of critical path replica or standard inverter chain is monitored [3], [4]. Because of the monitors digital nature, the variation can be monitored easily by comparing the delay to clock period. However, this approach has two problems under large process variation and lower supply voltage. One is that critical paths change depending on a process/voltage/temperature (PVT) condition. Another is the increase of leakage current under unbalanced P/N-ratio variation. To solve the first problem, tunable replica critical path or representative critical path are proposed [5], [6] which has large area and design overhead. The second problem occurs for "SF" (slow nMOSFET and fast pMOSFET) and "FS" corners where uniform P/N biasing causes large leakage overhead, which will be demonstrated in the next section.

Leakage monitoring is used to monitor MOSFET performances [2]. Leakage monitoring enables to detect P/N variation independently and allow optimal performance compensation. However, leakage monitor circuits are analog and thus the design of monitor and control circuitry has large design and area overhead.

This paper proposes digital monitor circuits to detect P/N variations. P/N-sensitive inverter structures are developed whose delay becomes sensitive to either nMOSFET or pMOSFET performance. Thus, conventional delay based compensation technique can be used but with independent controllability over nMOSFET and pMOSFET. This controllability can save a large leakage overhead as will be shown in a later section of the paper. Besides, critical path replica or synthesis of critical paths are not required in the monitor circuits. As the proposed scheme is not dependent on the critical paths, they can be ported across product and process without extra design cost.

Using the proposed monitor circuits, a built-in self-adjustment (BISA) scheme is developed to adjust MOSFET performances to the target values with adaptive body bias. MOSFET performances are adjusted automatically by comparing the monitor delay to the clock signal. Well voltages are generated dynamically according to the monitored MOSFET performances. System supply voltage and clock are used to generate body voltages. Thus, no external supply voltage or I/O port is required.

The contributions of the paper are as follows.

1) Develop P/N-sensitive digital monitor circuits.
2) Develop built-in self-adjustment scheme which adjusts MOSFET performances to the target values.
3) Validation from corner chip measurements.

The remainder of the paper is organized as follows. In Sec. II, schematic of the proposed monitor cell and its sensitivity to MOSFET performance is explained. In Sec. III, design procedure of BISA is described. A test chip has been fabricated in a 65 nm process to validate the proposed technique. Test chip design procedure is explained in Sec. IV. Measurement results of several corner chips are demonstrated in Sec. V. Finally, Sec. VI concludes the paper.

II. Digital P/N-sensitive Monitor Cells

First, the importance of controlling nMOSFET and pMOSFET independently will be demonstrated. Fig. 1 shows simulated frequency of a 2-input NAND gate ring oscillator (RO) and leakage current of a conventional LSI for an unbalanced P/N corner ("SF") along with a balanced corner ("TT"). A commercial 65 nm transistor model is used here. We can observe that frequency decreases and leakage increases at "SF" corner. If we apply forward body bias for both the nMOSFET and pMOSFET uniformly to compensate circuit speed to "TT" value, the leakage current increases by 16 times which is

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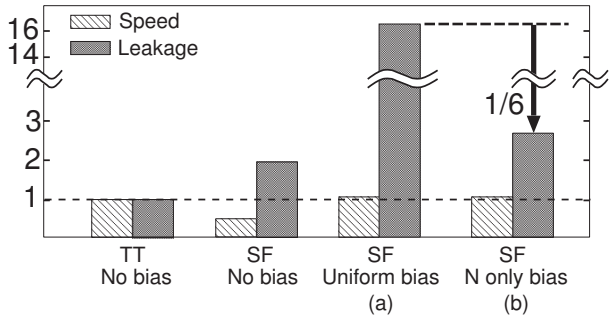
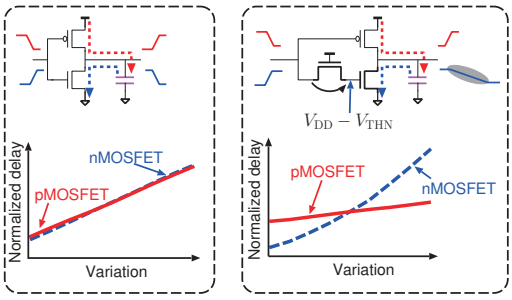


Fig. 1. Circuit speed and leakage for two corners of "TT" and "SF". Forward body bias is applied for "SF" corner to compensate speed based on (a) critical path monitoring (uniform bias) and (b) P/N-sensitive monitoring (N only bias).



(a) Conventional logic cell (b) Variation-sensitive monitor cell

Fig. 2. Sensitivity of the proposed monitor cell compared to conventional logic cells. The proposed monitor cell is sensitive to a particular type of MOSFET variation only.

unacceptable especially for mobile devices. However, if we apply forward body bias to the slower device only, which is nMOSFET in this case, the leakage overhead is only 2.6 times, which means 6 times leakage saving can be achieved than the conventional method of uniform biasing. Thus, adaptive biasing based on independent nMOSFET and pMOSFET variations is required for superior power characteristics.

In this paper, new digital monitor cells are developed which becomes particularly sensitive to either pMOSFET or nMOSFET variation. Fig. 2 shows the proposed nMOSFET-sensitive monitor cell structure along with the conventional inverter structure. An nMOSFET pass-gate is inserted in between the input port and the nMOSFET of the inverter structure for nMOSFET-sensitive monitor cell. This structure makes the fall delay 4 times larger than the rise delay at 0.7 V operation. The use of pass-gate for enhancement of variation effects are used in [7], [8]. The conventional approach is to use the pass-gates at the output of the inverter. However, conventional structure enhances the variation effects of both P/N because of the voltage drop across the pass-gate. For the proposed structure in Fig. 2, the voltage drop only affects the nMOSFET of the inverter, thus the delay becomes sensitive to nMOSFET variation only. Sensitivities of rise and fall delays to MOSFET threshold voltage variations are shown in the figure. The fall delay of monitor cell in Fig. 2(b) is highly sensitive to nMOSFET variation whereas the rise delay has very less sensitivity to pMOSFET variation. Similarly, pMOSFET sensitive monitor cell can be designed. The proposed monitor cells are very simple to design and can be used in the standard cell-based design flow.

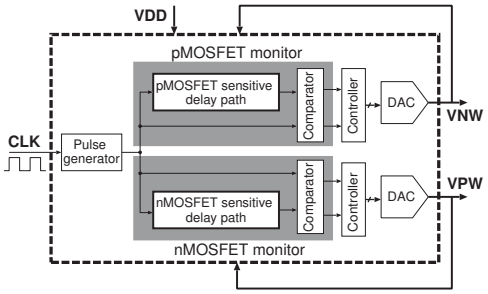


Fig. 3. Schematic of built-in self-adjustment scheme. P/N variations are detected comparing the clock with the delays of monitor paths. System supply and clock is used to generate body voltages.

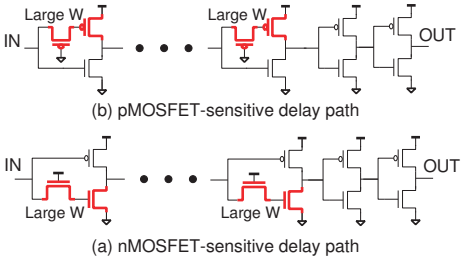


Fig. 4. Proposed variation-sensitive monitor circuit structure. Pass-gate at input makes the delay highly sensitive to MOSFET variation.

III. Built-in Self-adjustment Scheme

Using the digital monitor cells proposed in Sec. II, a simple BISA scheme is developed with small area overhead.

A. Basic Concept

The basic concept is to detect MOSFET variations by comparing the delays of P/N-sensitive monitor paths to clock period. If the delay is larger than the clock period, MOSFET performance is lower than the target and vice-versa. The number of stages are determined so that the delay is the same as the clock period at "TT" corner. As clock is used as the reference, no external reference voltage is required. Once the delays achieve the target delays, the system goes to stable condition. A comparator generates up/down signals which is then translated into digital codes by a controller. Finally, DAC will convert the digital value to analog value. During the stable condition, generated well voltages will fluctuate by LSB of controller output.

B. Overall Schematic

The schematic of BISA scheme is illustrated in Fig. 3. During the stable condition, comparison between delay path and clock signal is not required with high frequency. This allow us to reduce dynamic power by decreasing the comparison frequency. A pulse generator is used instead of the clock signal itself to achieve this. Pulses are generated once in every 1024 cycles. The delays are compared with the generated pulse width. Pulse width is made longer than the original clock period so that the number of stages for delay paths can be increased to reduce random variation effect. Delay $T_{\rm mon}$ of the monitor is set to be $T_{\rm mon} = T_{\rm pulse} + \alpha$ where $T_{\rm pulse}$ is the pulse width and α is for guard band. A phase comparator

Table I
COMPARISON BETWEEN DIFFERENT MONITOR CIRCUITS.

	Sensitivity	P/N monitoring	Calibration	Design overhead
Leakage [2]	**High**	**Yes**	Analog	High
Critical path [3]	Low	No	**Digital**	**Medium**
Proposed	**High**	**Yes**	**Digital**	**Low**

detects the phase difference between the delayed pulse and the input pulse, and generates up/down signals.

C. Delay path design

Fig. 4 shows the delay paths to monitor pMOSFET and nMOSFET variations where monitor cells described in Sec. II are used. In order to reduce random variation effect, gate widths for the sensitive MOSFETs are made 4 times than those in the standard cells. Standard inverter cells are used at the last few stages to reshape the waveform. Table I shows the comparison between different monitor circuits.

Target operation for the chip is set to $V_{\rm dd} = 0.7$ V and clock frequency ($f_{\rm clk}$) of 40 MHz. The delays of the monitor circuits are set to 27 ns which is slightly larger than the clock period of 25 ns.

D. Comparator and Controller

Conventional PFD (Phase Frequency Detector) is used to detect the phase difference between the outputs of the P/N-sensitive delay paths and the input pulse. The PFD generates up/down signals which is fed to the controller. The controller consists of 6-bit counter which counts the up/down signals. When the up signal is high, the counter value goes up and the down signal is high the counter value goes down. The counter values are then fed to the DACs which generate well voltages.

E. DACs

Forward body bias is implemented in our design for demonstration. However, reverse body bias can be easily adopted with the proposed monitor circuits as well. A charge-redistribution based DAC is designed in this scheme for area-efficiency. The details of the DAC design is left for future discussion.

IV. TEST CHIP DESIGN

A test chip has been fabricated in a 65 nm process to demonstrate the validity of BISA scheme. Fig. 5 shows the chip photograph and layout of BISA. In order to measure gate speeds, ROs are integrated in the target substrate area. ROs consist of standard inverter (INV), 2-input NAND gate and 2-input NOR gate. ROs consisting of the proposed monitor cells are also designed to monitor process variation directly. Additional test circuits are implemented to observe the internal states of the controller, DACs and well voltages. Total area of BISA excluding test circuits is 2564 μm^2. Target area for self-adjustment is set to be 0.1 mm^2. Area overhead is 2.6%.

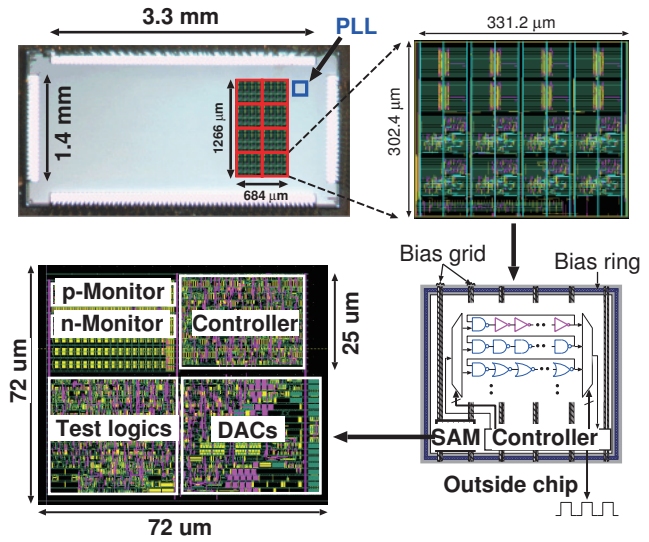


Fig. 5. Chip photograph and layout of the self-adjustment scheme. ROs of several logic gates are implemented to evaluate critical path delays.

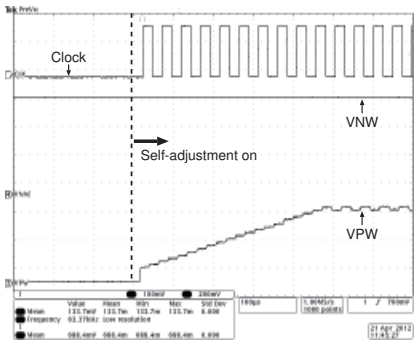


Fig. 6. Measured transient response of the self-adjusting module when self-adjustment is enabled. System stability and independent control of body bias is confirmed.

V. MEASUREMENT RESULTS

Test chips have been fabricated targeting "TT" condition, as well as four corners of "SS", "FF", "FS" and "SF". In this section, first we show that the proposed monitor circuits can detect P/N variations correctly. Next, we show that the well voltages are generated according to the monitored variations. Finally, speed compensation results for different logic gates and corresponding leakage current will be presented. All the measurements are done at $V_{\rm dd} = 0.7$ V.

A. Transient Response

Transient response of the system is measured when self-adjustment is enabled. Fig. 6 shows measured transient response for "SF" corner. After self-adjustment is enabled, body voltage of nMOSFET (VPW) is gradually increased until the delay of nMOSFET monitor is smaller than the target value. pMOSFET body voltage remains constant as pMOSFET is faster than the target performance. Thus, independent control of nMOSFET and pMOSFET is confirmed.

B. Monitor Outputs and Body Voltage Measurements

Fig. 7 plots the output frequency of pMOSFET-sensitive RO against the output frequency of nMOSFET-sensitive RO to

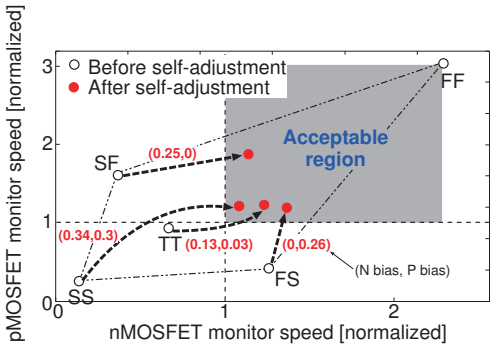


Fig. 7. Output performances of pMOSFET-sensitive and nMOSFET-sensitive ROs. Performances are measured before and after self-adjustment. Generated body biases for each corner are shown in closed bracket.

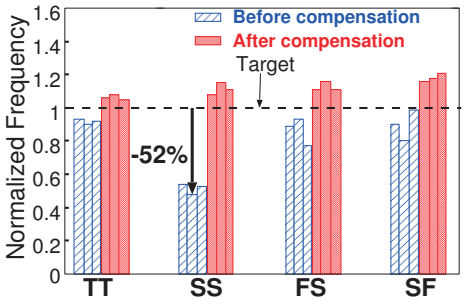


Fig. 8. Frequencies of ROs consisting of various kinds of gates. INV, NAND and NOR frequencies are plotted for each corner from the left.

illustrate the corner conditions. Speeds are normalized by their target values. Open circles show the measured values before self-adjustment and closed circles show the values after self-adjustment. Generated body biases for each corner are also shown. Maximum of 0.34 V body bias was required to adjust speed at "SS" corner. After self-adjustment, the "SS" chip is moved to a point where the speeds of both monitors are above the target values. Similarly, "SF", "TT" and "FS" chips are also moved so that the target speeds are achieved.

C. Speed Measurement

Speeds of different gates are measured through RO frequencies as they are the most concern. Fig. 8 shows the values of INV, NAND and NOR RO frequencies for all the corner chips. Frequencies before and after self-adjustment are shown. The values are normalized by the target values. The worst case speed degradation here is -52% at "SS" corner. After self-adjustment, the frequencies go over the target values. For "FS" and "SF" corner chips, variations among the gate speeds become significant as pMOSFET and nMOSFET move to opposite directions. After self-adjustment, all the gates achieve the target speeds.

D. Leakage Measurement

Leakage currents are measured before and after self-adjustment. Two types of self-adjustment is compared to demonstrate the need for P/N-sensitive monitors. One is the conventional critical path delay based adjustment using uniform biasing, another is the proposed one. Fig. 9 shows the leakage currents for "TT", "SF" and "FS" corners. 2.6 times

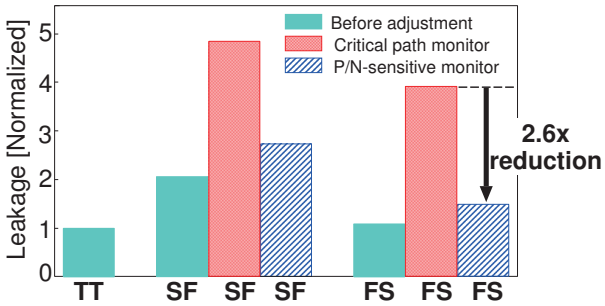


Fig. 9. Leakage measurement for "TT", "SF" and "FS" chips when (a) both MOSFETs are biased uniformly and (b) proposed scheme is applied.

leakage saving is achieved by using the proposed monitor circuits than the conventional critical path based method.

VI. Conclusion

A simple built-in self-adjustment (BISA) circuit is developed to adjust P/N performances to their target values. An all-digital monitor circuit is developed which is capable of detecting nMOSFET or pMOSFET variation. Measurements from several corner chips show the validity of the proposed circuit. Self-adjustment of P/N performances is confirmed. Performance measurements of logic gates confirm more than 50% of speed recovery at 0.7 V operation. 2.6 times leakage saving is achieved compare to the conventional critical path based method using uniform biasing. The scheme is suitable for typical-case design and yield enhancement.

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