Extraction of Variability Sources from Within-die Random Delay Variation

Shuichi Fujimoto*, Islam A.K.M Mahfzul*, Shinichi Nishizawa*, and Hidetoshi Onodera*,§

*Dept. Communications and Computer Engineering, Kyoto University, Japan

Abstract—Characterization and modeling of delay variability on a real silicon is a key topic for statistical timing analysis. In this paper, we propose a method of extracting variability information from a real silicon. We have measured WID delay variability in 65nm process using RO-array test structures, and discuss how to separate random component into the variability of threshold voltage and channel length.

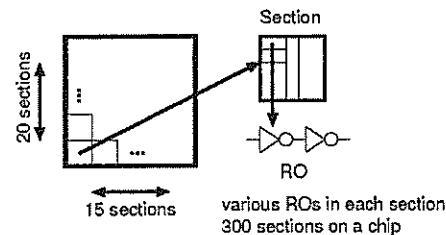Keywords: delay variability, RO-array, WID variation, SSTA, variation modeling

I. INTRODUCTION

With the progress of technology scaling, variability becomes a serious issue in LSI design. In the present and the future, intrinsic atomistic variations such as random dopant fluctuation and line edge roughness become prominent[1], resulting in within-die[WID] random variation that requires statistical treatment in performance analysis. While there are extensive studies and remarkable achievements have been accomplished in the theoretical aspect of statistical performance analysis[2][3], another key challenge is the characterization of WID variation that appears on a real silicon.

Without accurate variability information that highly correlates with silicon, we cannot estimate or simulate performance variability of the circuit under design. We therefore need a method for obtaining the amount of variation appears in device parameters such as threshold voltage and channel length from the measured variability of test structures.

A possible method is to use a device-array test structure and measure the variability of each transistor performance and physical structure[4]. This is the most basic method but it requires huge amount of cost in chip fabrication, measurement, and analysis. Also, the layout structure of an device-array is very much different from that of a real circuit which is basically an array of primitive gates.

In order to develop a systematic method that can be applied to various fabrication processes for providing accurate variability information required by statistical design methodologies, we have developed an RO-array test structure and an analysis method for characterizing WID variability[5][6]. We have decomposed the measured WID variation into three components of random, deterministic, and systematic, where random component is the largest at a transistor level. Details of the decomposition are explained in a separate paper presented in this workshop[6]. In this paper, we will explain how we can derive the variability of threshold voltage and channel length from the variability of measured oscillation frequencies. Extracted amount of variation can be readily used in statistical simulation such as Monte Carlo analysis.

The reminder of this paper is organized as follows. In Section II, we briefly explain our RO test structure and measured WID random variability under different supply voltages.
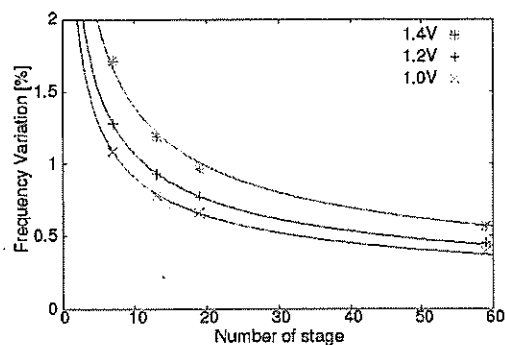

Fig. 1. 65nm Test Structure

Fig. 2. The amount of random component vs. stage-length

Threshold voltage and channel length, which are major sources of variability, have different supply-voltage dependencies of variability. Exploiting this difference, we propose a method for extracting the amount of variation in channel length and threshold voltages of PMOS and NMOS transistors. In Section III, we will show the result of the extraction in a 65nm process and explain how the extracted variation can reproduce measured performance variability by Monte Carlo simulation. Finally, Section IV summarized this paper.

II. CHARACTERIZATION OF DELAY VARIABILITY

A. An RO-array test structure and measured random WID variation

We have measured WID variability using an RO-array test structure. A simplified structure of the test chip is shown in Fig. 1. A "Section" that contains several tens of different ROs is regularly placed in a 15-by-20 array, resulting 300 identical ROs over a die. By measuring oscillation frequencies of 300 identical ROs, we can obtain WID frequency variation. The WID variation is then decomposed into random, deterministic, and systematic components. Detailed explanation of the test structure and the decomposition method as well as statistical
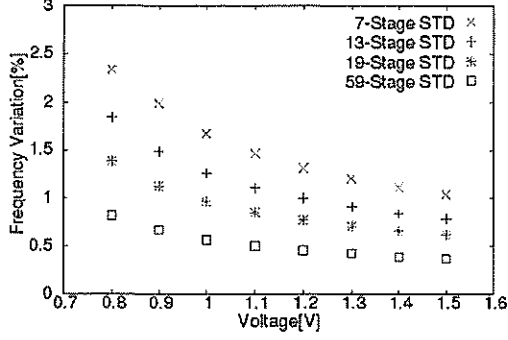
Fig. 3. Random Variation (STD RO)

Fig. 4. Ring Oscillator (7-Stage)

Fig. 5. Voltage dependency of sensitive parameter (13-stage standard RO)

properties of the three components can be found in a separate paper presented in this workshop[6]. The random component is purely random without spatial correlation and it is the dominant component at a transistor-level. In this study, we further estimate the origin of WID random variability.

In this section, we show an example of the measured WID frequency variation obtained in a 65 nm test structure. Fig. 2 shows the amount of random WID variation in ROs composed of inverters as a function of the number of stages under three different supply voltages. The stage-length dependency in Fig. 2 obeys $1/\sqrt{n}$ relations that support the randomness of the measured WID random variability. Fig. 3 shows the WID random variation of four ROs as functions of supply voltages. The variability rapidly increases when the supply voltage decreases into sub-1V region. We will use this supply-voltage dependencies for the decomposition of of the WID random variation.

B. Extraction of WID random variation

We estimate the origin of WID variability on real silicon. For simplicity, we assume the sources of variability are limited to channel length L and threshold voltages of pMOSFET and nMOSFET. They are main factors of changing transistor current[7] that directly affects oscillation frequency. Threshold voltage has a channel length dependency due to short channel effects and hence its variation consists of two components. One component correlates with channel length variation. The other component is random and it does not correlate with channel length variation. The latter component corresponds to a variation in long-channel threshold voltage which, for example, is represented by parameter $VTH0$ in BSIM4 model[8]. We therefore estimate the amount of three independent random components that originate from channel length L, long-channel threshold voltage of pMOSFET V_{thP}, and that of nMOSFET V_{thN}.

Those sources lead to different supply-voltage dependency of variability. For example, threshold voltage variation results in relatively larger delay variability in lower supply voltage, whereas channel length variation does not so much.

Assuming linear sensitivity of each variability source, the variability of oscillation frequency is given in the equation below.
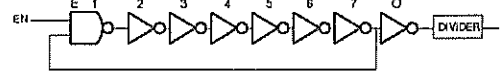
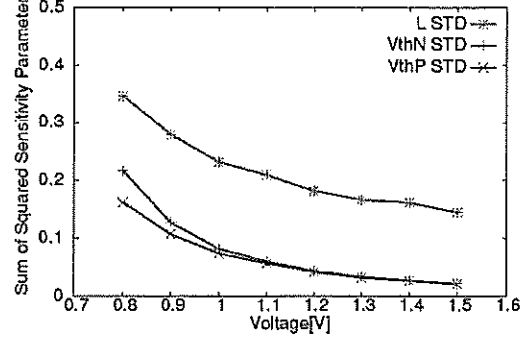$$\left(\frac{\sigma_f}{\mu_f}\right)^2 = \sum_i \left(k_{V_{thPi}}^2 \left(\frac{\sigma_{V_{thP}}}{\mu_{V_{thP}}}\right)^2 + k_{V_{thNi}}^2 \left(\frac{\sigma_{V_{thN}}}{\mu_{V_{thN}}}\right)^2 + k_{L_i}^2 \left(\frac{\sigma_L}{\mu_L}\right)^2\right) \quad (1)$$

In Eq.(1), $k_{V_{thPi}}$, $k_{V_{thNi}}$, and k_{L_i} are the sensitivity parameters for V_{thP}, V_{thN} and L variation, respectively. Parameters μ_f, $\mu_{V_{thP}}$, $\mu_{V_{thN}}$, and μ_L represent mean values of oscillation frequency, V_{thP}, V_{thN}, and L, respectively. Parameters σ_f, σ_{VthP}, σ_{VthN}, and σ_L are standard deviations of oscillation frequency, V_{thP}, V_{thN}, and L, respectively. Index i identifies an inverting gate in a ring-oscillator as shown in Fig. 4. Due to a NAND2 gate for controlling oscillation, each inverter has slightly different contribution to oscillation. Therefore we derive $k_{V_{thP}}$, $k_{V_{thN}}$, and k_L for each pair of transistors by numerical differentiation through circuit simulation[9]. For example in the circuit in Fig. 4, we derive 27 sensitivity parameters in total. The process condition for the sensitivity analysis, which is represented by the value of $\mu_{V_{thP}}$, $\mu_{V_{thN}}$ and μ_L is derived by the method described in Ref.[10] and hence the simulated oscillation frequency with $\mu_{V_{thP}}$, $\mu_{V_{thN}}$ and μ_L matches the measured mean oscillation frequency.

In this equation, we can measure $\left(\frac{\sigma_f}{\mu_f}\right)^2$. Unknown parameters that we want to derive are $\left(\frac{\sigma_{V_{thP}}}{\mu_{V_{thP}}}\right)^2$, $\left(\frac{\sigma_{V_{thN}}}{\mu_{V_{thN}}}\right)^2$, and $\left(\frac{\sigma_L}{\mu_L}\right)^2$. If we have at least 3 equations with different set of $k_{V_{thP}}$, $k_{V_{thN}}$, and k_L, we can derive the unknown parameters of our interest.

We exploit different voltage dependencies of those parameters to derive enough number of relations expressed in Eq.(1). Fig. 5 shows the amount of $\sum k_{V_{thPi}}^2$, $\sum k_{V_{thNi}}^2$, and $\sum k_{L_i}^2$ as functions of supply voltages for the circuit shown in Fig. 4. Sensitivities of L and threshold voltages (V_{thP} and V_{thN}) are very much different. However, the sensitivity of $k_{V_{thP}}$ and $k_{V_{thN}}$ are similar and it is very difficult to distinguish those two sources. We should need another circuit that has different performance sensitivities for V_{thP} and V_{thN}. An example is an inverter with an nMOSFET pass transistor at the output node as shown in Fig. 6. An RO with this circuit as an
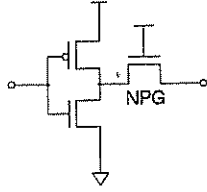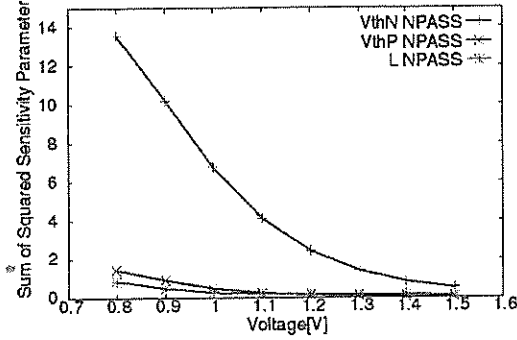
Fig. 6. NMOS Passgate

Fig. 7. Voltage dependency of sensitive parameter (13 stage pass-transistor-loaded RO)

TABLE I
EXTRACTED WID VARIABILITY σ/μ

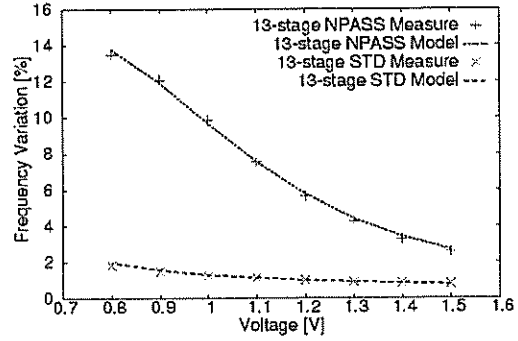| Random	V_{thP}	V_{thN}	L
$\sigma/\mu[\%]$	1.20	3.71	1.38

Fig. 8. Comparison of Model with Measurement

Fig. 9. Model of other RO structure

Fig. 10. Comparison of Model with Monte Carlo Simulation

oscillation element is sensitive to V_{thN} [11] and hence we have different sensitivities for V_{thP} and V_{thN}. Fig. 7 shows the sensitivities of a 13 stage pass-transistor-loaded RO as functions of supply voltage. This circuit is very sensitive to the threshold of nMOSFET.

III. MEASUREMENT AND ANALYSIS OF RANDOM COMPONENT

In this section, we show the result of variability decomposition. We select a 13-stage inverter RO and a 13-stage pass-transistor-loaded inverter RO for deriving variability of V_{thP}, V_{thN}, and L. WID oscillation variation of two ROs are measured in the supply voltage of 0.8 to 1.5 V, as shown in Fig. 8. We applies a least-square method for deriving the amount of variations in V_{thP}, V_{thN}, and L. Extracted WID variations are listed in Table 1. In this process, the long-channel nMOSFET threshold voltage has more than 2 times larger variation than the long-channel pMOSFET threshold voltage. Estimated frequency variation by Eq.(1) based on the extracted variations are also listed in Fig. 8. Good agreement can be seen. Fig. 9 shows measured WID random variations for other RO and estimated variation by Eq.(1). They are in good agreement.

The threshold variability listed in Table 1 represents the variability of long-channel threshold voltage. As explained in Section II, another source of threshold variability is channel length variation. Accommodating both sources of variation, we calculate the total variability of threshold voltage at V_{dd} = 1.2V. Variability increases to 1.81% and 3.77% for pMOSFET and nMOSFET respectively.

Finally, we examine the accuracy of linearized variability model of Eq.(1). Using the extracted variability of V_{thP}, V_{thN}, and L, we run Monte Carlo circuit simulation for a 13-stage inverter RO and a 13-stage pass-transistor-loaded RO and
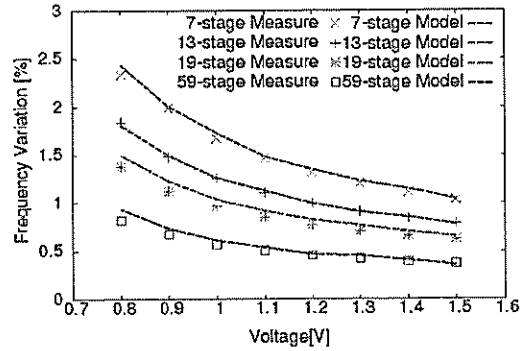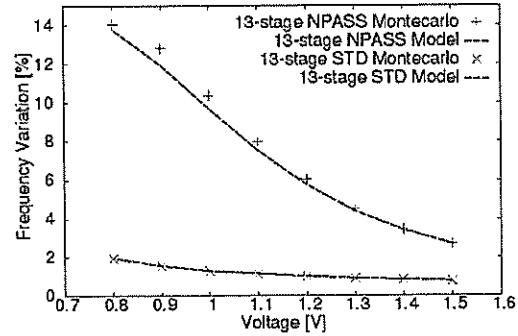
compare the result with the variability estimated by Eq.(1). The comparison is shown in Fig. 10. Frequency variation obtained by Monte Carlo simulation is consistently higher than Eq.(1). but the discrepancy is less than 3.1% for this level of small variation. We thus rely on the linear model of Eq.(1) for the decomposition of variability sources.

IV. CONCLUSION

In this paper, we explain a method for decomposing WID random variation into the variability of channel length and threshold voltage of an nMOSFET and a pMOSFET. We measured WID random variability of RO-array structures under different supply voltages and separated random component into variation of V_{thP}, V_{thN}, and L. Extracted (σ/μ) of V_{thP} is 1.20%, V_{thN} is 3.71%, and L is 1.38%. In the study, we focus on three sources of variability. Investigation of other source of variability is underway.

REFERENCES

[1] A. Asenov, A.R. Brown, J.H. Davies, S. Kaya, and G. Slavcheva. Simulation of intrinsic parameter fluctuations in decananometer and nanometer-scale mosfets. *Electron Devices, IEEE Transactions on*, Vol. 50, No. 9, pp. 1837 – 1852, sept. 2003.

[2] Brian Cline, Kaviraj Chopra, David Blaauw, Andres Torres, and Savithri Sundareswaran. Transistor-specific delay modeling for ssta. In *DATE '08: Proceedings of the conference on Design, automation and test in Europe*, pp. 592–597, New York, NY, USA, 2008.

[3] H. Chang, V. Zolotov, S. Narayan, and C. Visweswariah. Parameterized block-based statistical timing analysis with non-gaussian parameters, nonlinear delay functions. In *Design Automation Conference, 2005. Proceedings. 42nd*, pp. 71 – 76, june 2005.

[4] T. Tsunomura, A. Nishida, F. Yano, A.T. Putra, K. Takeuchi, S. Inaba, S. Kamohara, K. Terada, T. Hiramoto, and T. Mogami. Analyses of 5σ vth fluctuation in 65nm-mosfets using takeuchi plot. *VLSI Technology, 2008 Symposium on*, pp. 156 – 157, June. 2008.

[5] H.Onodera and H.Terada. Characterization of wid delay variability using ro-array test structures. In *3rd IEEE International Workshop on Design for Manufacturability & Yield*, pp. 15–19, 2009.

[6] S. Nishizawa, K. kobayashi, and H. Onodera. Variability characterization using an ro-array test structure and its impact on design. *IEEE DFM&Y Workshop*, June 2010.

[7] R.Newton T.Sakurai. Alpha-power law mosfet model and its applications to cmos inverter delay and other formulas. In *IEEE Journal of Solid-State Circuits*, pp. 584–594, 1990.

[8] INC. Meta-Software. *BSIM4.3.0 MOSFET Model - User's Manual*, 1996.

[9] *HSPICE User's Manual:Simulation and Analysis*, 2003.

[10] Islam A.K.M Mahfuzul, K. kobayashi, and H. Onodera. Process-sensitive monitor circuits for estimation of die-to-die process variability. *TAU Workshop*, March 2010.

[11] M. Bhushan, A. Gattiker, M.B. Ketchen, and K.K. Das. Ring oscillators for CMOS process tuning and variability control. *Semiconductor Manufacturing, IEEE Transactions on*, Vol. 19, No. 1, pp. 10–18, 2006.